ULVAC IR Seminar 2025

Aiming for Further Growth in the Semiconductors and Electronics Field

October 3, 2025

Disclaimer regarding forward-looking statements etc.

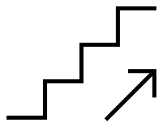
- **Forward-looking statements**
  Forward-looking statements of the company in this presentation are based on information that was available at the time these documents were prepared. There are several factors that directly or indirectly impact the company performance, such as the global economy; market conditions for FPDs, semiconductor, electronic devices, and raw Materials; trends in capital expenditures and fluctuations in exchange rates. Please note that actual business results may differ significantly from these forecasts and future projections.
- **About This Document**
  Please note that this IR seminar material and presentation were not created for technical purposes and contain simplifications to facilitate investor understanding.

Growth Strategy

Selection and concentration of a business portfolio centered on semiconductors and electronics

- Accelerate focus on Semiconductors and Electronics
- Create new semiconductors and electronics-related businesses by leveraging synergies among businessses
- Expand business through M&A and other initiatives

Approx. ¥110 billion increase



Consolidated net sales improvement by FY31/6

Today's Agenda

1 **Initiatives for Semiconductor Process Expansion**

16:05-16:20

Tomoyasu Kondo, Senior Executive Officer,
General Manager of Semiconductor Equipment BU

2 **New Initiatives in Advanced Packaging**

16:20-16:35

Harunori Iwai, Senior Executive Officer
Junya Kubo, Sales Department 2
Semiconductor and Advanced Electronics Business HQ

3 **Strengths of the Surface Analysis System and Future Developments**

16:35-16:50

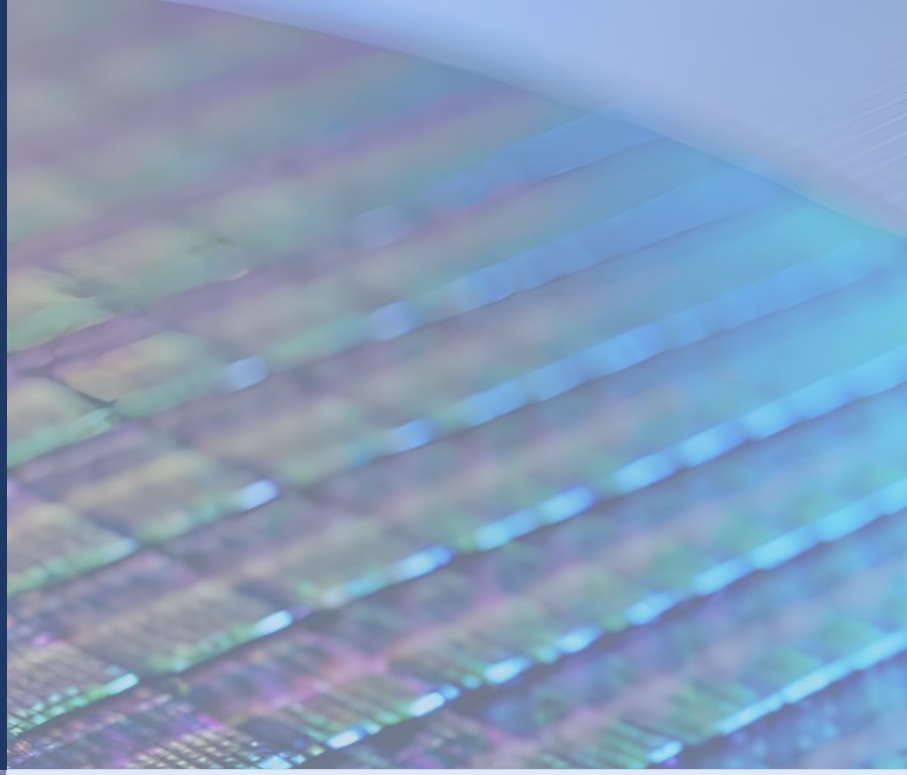
Hirohisa Takahashi, Executive Officer,
President and CEO of ULVAC-PHI, Inc.
Takuya Miyayama, Senior Manager,
Product Strategy Department, ULVAC-PHI, Inc.

4 **Q&A**

16:50-17:10

Initiatives for Semiconductor Process Expansion

Tomoyasu Kondo
Senior Executive Officer,
General Manager of Semiconductor Equipment BU



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Advanced Logic Foundry Technology Roadmap

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- New Mid-to-Long-Term Management Plan Over the six years through FY31/6, the significant structural changes to semiconductor devices will occur
- Increased patterning steps and adoption of new materials will expand opportunities for our core PVD deposition processes

	2022	2025	2026-	2028-	2030-	2032-
	N3	N2	A16/14	A10	A7	A5
BEOL	M0=23-26nm	M0=22nm	M0=21nm	M0=18-21nm	M0=18-20nm	M0=14-18nm
BEOL	M0 Cu SD			M0 DME Ru+AG	M0 Ru+AG AR3	M0-M3 Ru+AG AR3
MOL	W MOL				Mo/W MOL for CFET, Ru?	
FEOL	FinFET	Nanosheet	Nanosheet Scaling	Outer Wall Forksheet	CFET	CFET Scaling
Backside	BS-PDN				BS-PDN CFET	Back side Functional

Source: Created based on Imec Roadmap

Our Hard Mask Process Expansion and Application to Other Processes

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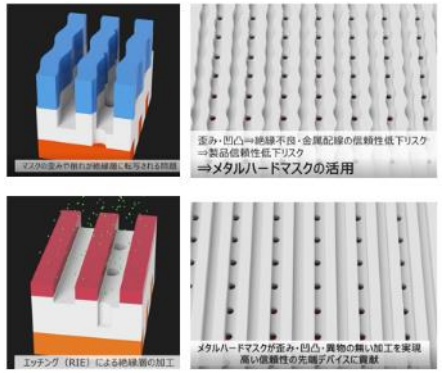
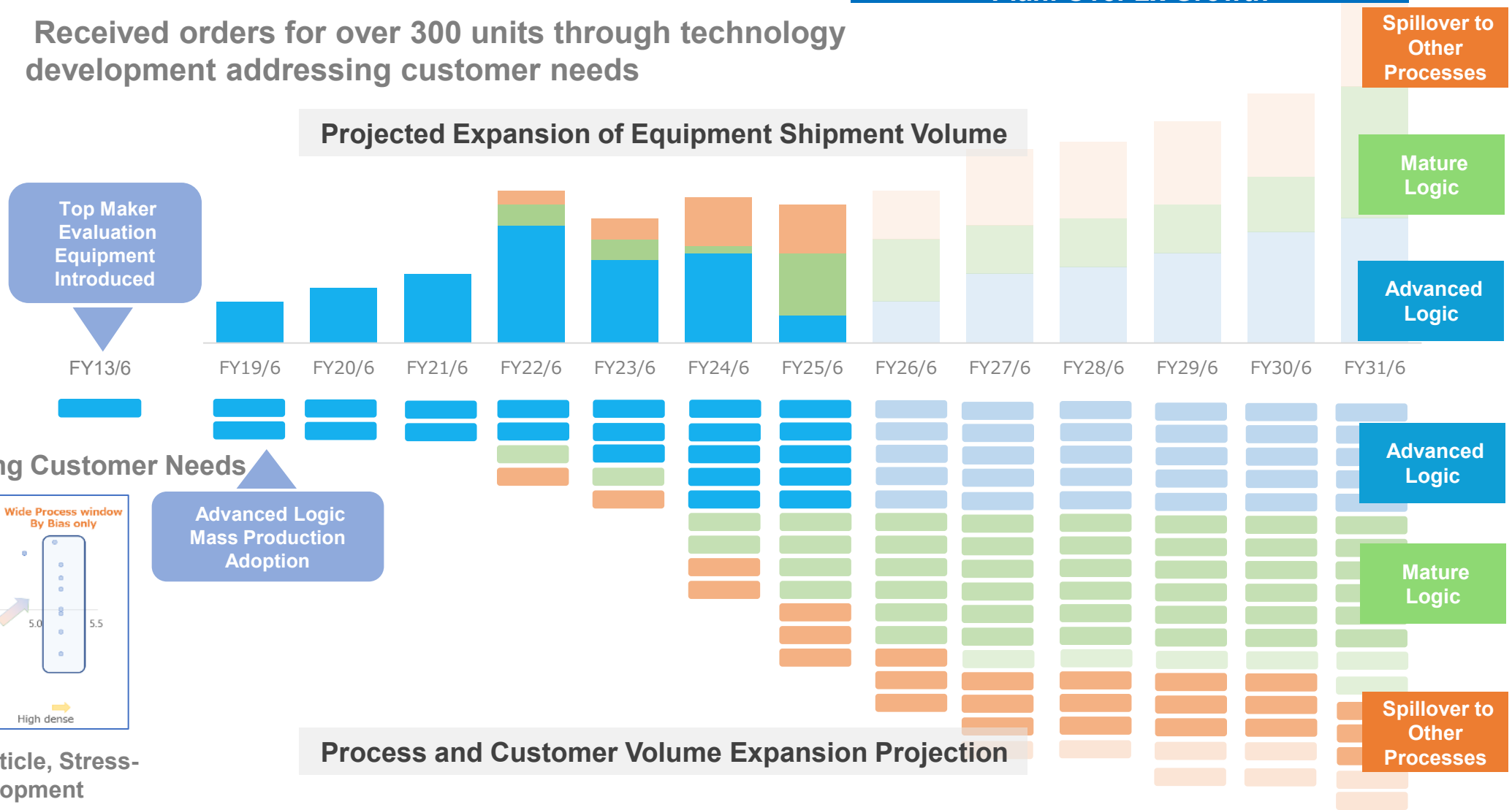
Technical challenges



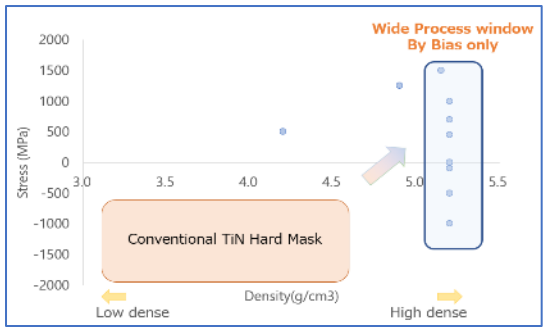
New Mid-to-Long-Term Management Plan: Over 2x Growth

Received orders for over 300 units through technology development addressing customer needs

Projected Expansion of Equipment Shipment Volume



Technology Meeting Customer Needs



High-Density, Low-Particle, Stress-Controlled MHM Development

Process and Customer Volume Expansion Projection

Spillover effects through securing mass production PORs with top customers

Technology application to other processes, process expansion

Our Advanced Semiconductor Development Framework

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» Strengthening Advanced Semiconductor Device Development: In addition to opening the Technology Center Pyeongtaek (Korea), we have commenced participation in the Imec program in Belgium. We are building a development framework with a forward-looking perspective

Advanced Customer Development Base

New

Advanced Semiconductor Research Institutions
(Participated in 2025)

Semiconductors and Electronics Technology Research Institute
(Established in 1990)

Technology Center Pyeongtaek
(Established in 2024)

~N+2	N+2 to N+1	N+1	N
Advanced Technology Sensing	Equipment Development	Customer JDP/JEP	Mass Production Feasibility and Yield Improvement
Development Collaboration	Process Development	Development POR/Mass Production POR	CS Support

Early sensing for sufficient lead time → Development Inquiry → Development Equipment Selection → Development → POR/Mass Production

Semiconductor & Logic Growth Roadmap

Technology Trends	Our Strengths
Progress in miniaturization	Stress control
Introduction of new materials	Low-particle film deposition
	Low-temperature film deposition technology

■ Growth Roadmap

Expansion of new materials and low-resistance film deposition technologies

Low-resistance new materials

☆ Proven track record

Acquisition of advanced logic metal wiring processes

Cu interconnect | Al/W Process

Hard mask technology development leveraging stress control and low-particle deposition

★Hard masks for BEOL wiring formation | ★Hard masks for GAA formation | Hard mask for back-side wiring formation

Customer Technology Roadmap	2024	2025	2026	2027	2028	2029	2030	2031
Logic	2nm		A14		A10		A7	

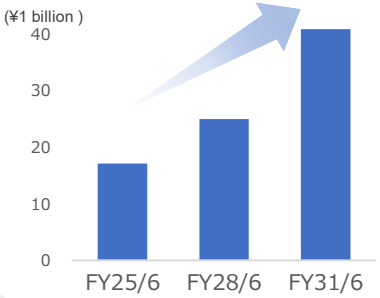
Mid- to Long-Term Goals

Hard Mask PVD+ Securing market share through the capture of the metal wiring process

- Centering on metal hard mask technology, which is the de facto standard at 5 nm and 3 nm, we aim to establish a market share in hard mask applications and related process technologies.
- Aiming to enter and expand into the metal wiring process, where PVD is most widely used

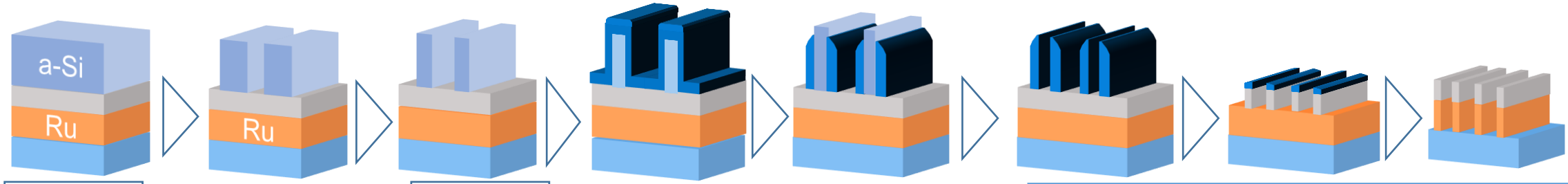
Orders Received

Approx. **2.4** x



An Example of Future Technology Development for Advanced Logic

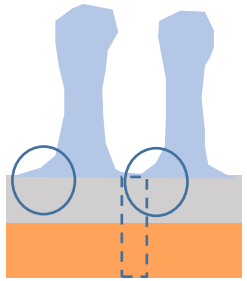
Example of hard mask applications in Ru DME processes



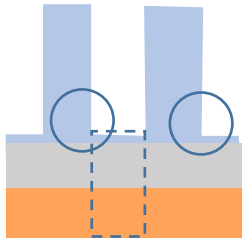
CVD

PVD

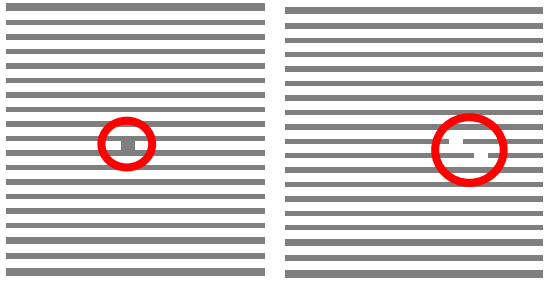
Shape distortion during trimming
Disadvantageous during pattern transfer



Density, Si purity, low deposition temperature, low outgassing
⇒Superior resistance to pattern distortion and pattern transfer



Effective against microbridges and defects



Amorphous Si: Comparison with PVD and CVD

	CVD	PVD
Deposition Temperature	High	Low
Purity	Low	High
Impurities (Hydrogen)	High	None
Hardness	Low	Mid
Film Thickness	thick	mid
Patterning accuracy	Bad	Moderate
Temperature tolerance	Moderate	High
Shape Retention	Low	Moderate
Film-forming particles	Will be Evaluated	

Sputtering Technology for Metal Wiring Processes: Logic

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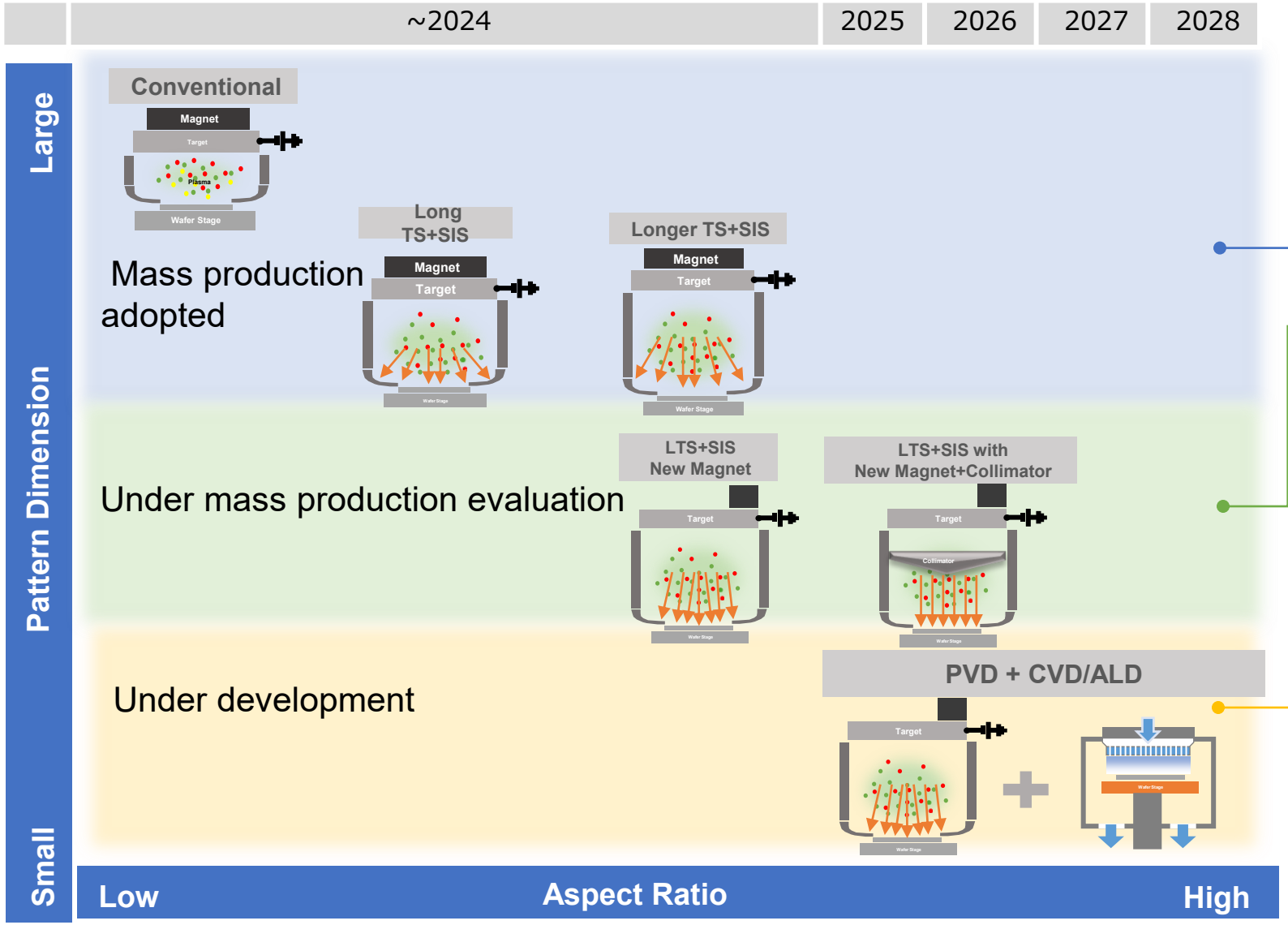
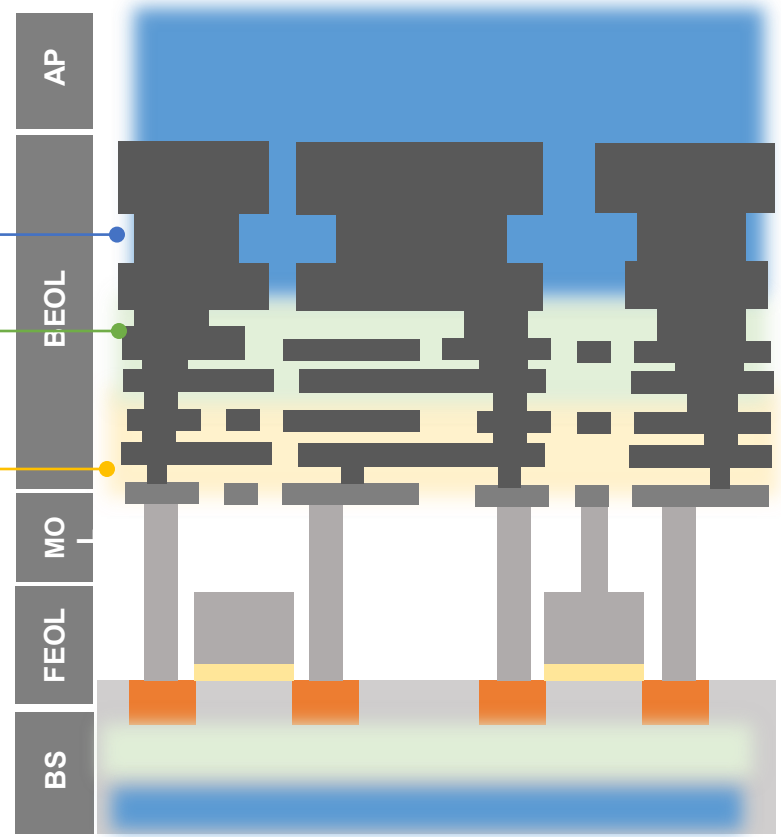
» Increased opportunities through miniaturization and multilayering of interconnect layers in the logic field





Semiconductor and Memory Growth Roadmap

Technology Trends	Our strengths
Progress in miniaturization	Low-particle film deposition
Acceleration of 3D structures	Stress control
Introduction of new materials	High-density film formation

■ Growth roadmap

CVD and ALD integration

Under development with leading memory manufacturers

Development of new materials and low-resistance film deposition technologies, and expansion of mid-process wiring

Cu bonding　　New Materials

☆ Proven track record

Expansion of cutting-edge memory processes such as　metal film processes and HM processes. and customer expansion

★ Cu, Al, W, and TiN wiring processes　　★ HBM wiring processes　　Back-side Film Deposition (Bonding, Stress Control)

Customer Technology Roadmap	2024	2025	2026	2027	2028	2029	2030	2031
DRAM	13nm	<12nm		<11nm		<10nm		
NAND	288L		3XX		4XX		4YY	

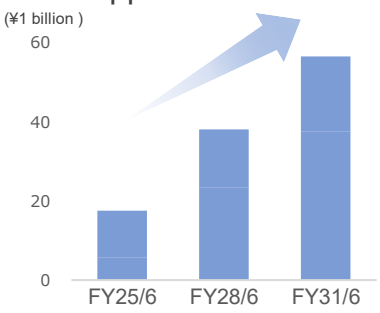
Mid- to Long-Term Goals

Maximizing market share in memory processes

- Accelerated joint development with a leading Korean manufacturer to expand the number of processes (utilizing the Technology Center)
- Expansion of processes through the provision of solutions compatible with new materials and structures

Orders Received

Approx. **3.6** x



Sputtering Technology for Metal Interconnect Processes - Memory

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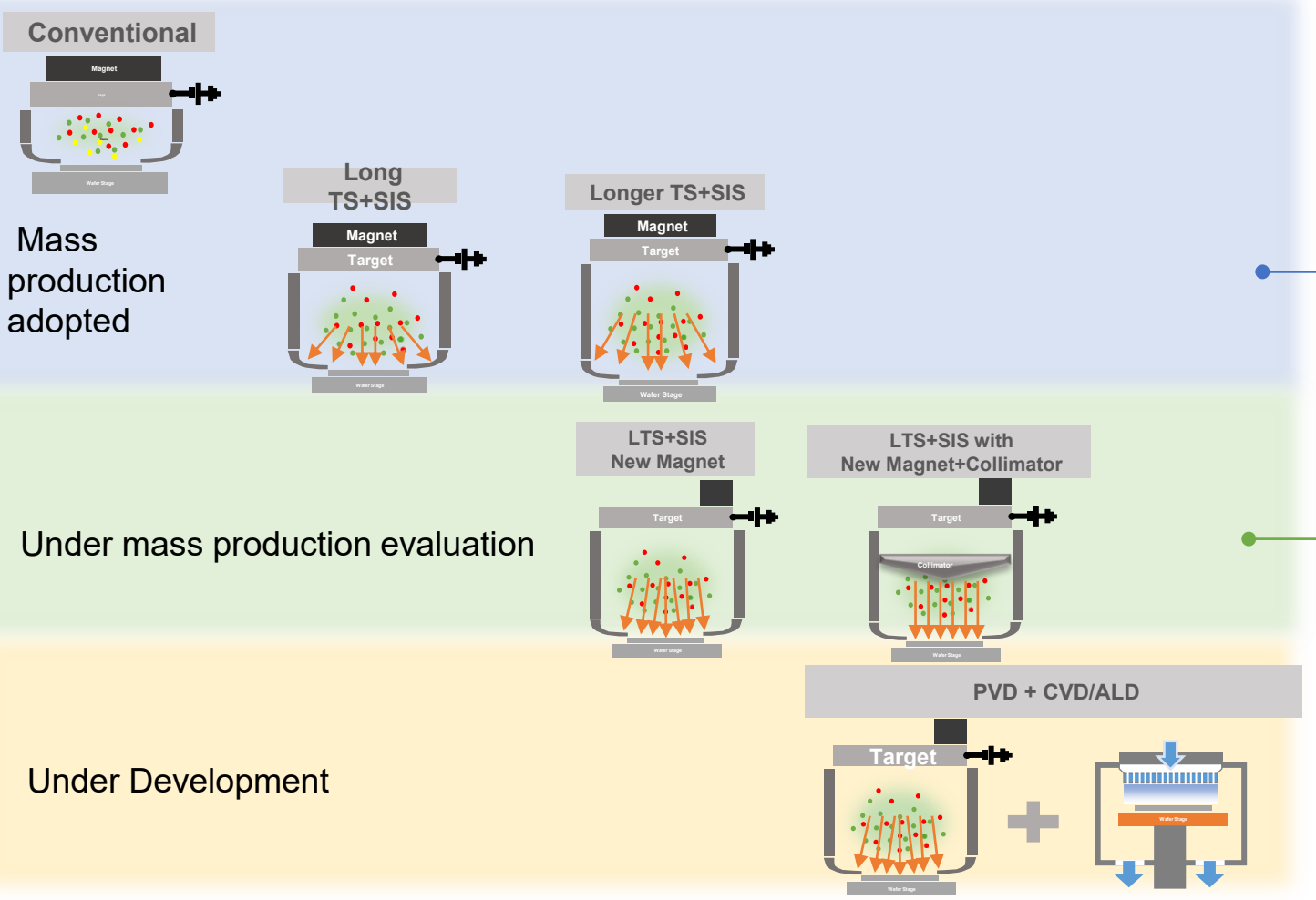
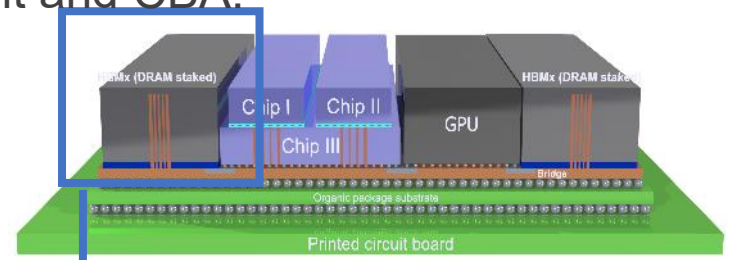
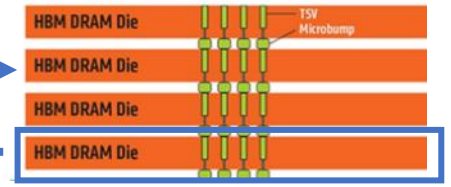
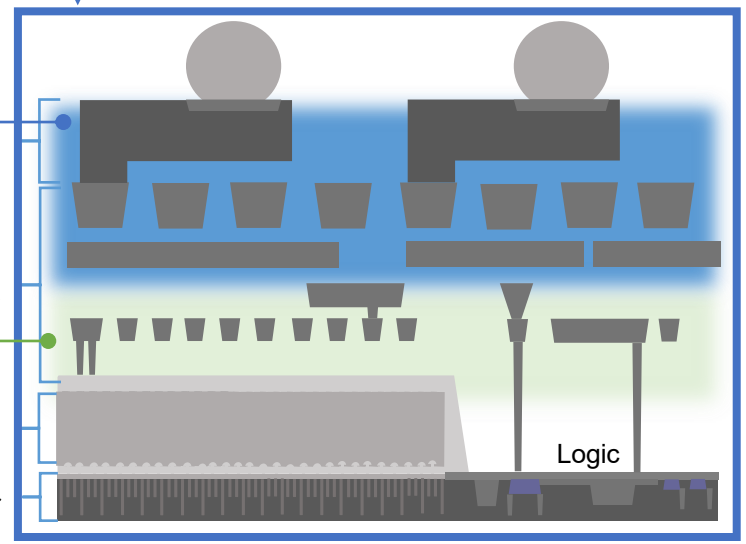
» Increased opportunities due to miniaturization and multilayering of interconnect layers in the memory field, along with the adoption of new structures such as increased total HBM count and CBA.

	～2024	2025	2026	2027	2028
Large	Conventional				
Pattern Dimension	Under mass production evaluation				
Small	Under Development				









Participation in the Imec Program and Future Collaboration

- We have participated in the program of Imec, a leading semiconductor research and development institute based in Belgium.
- By leveraging Imec's expertise and development infrastructure, we aim to accelerate the advancement of next-generation and beyond semiconductor devices.

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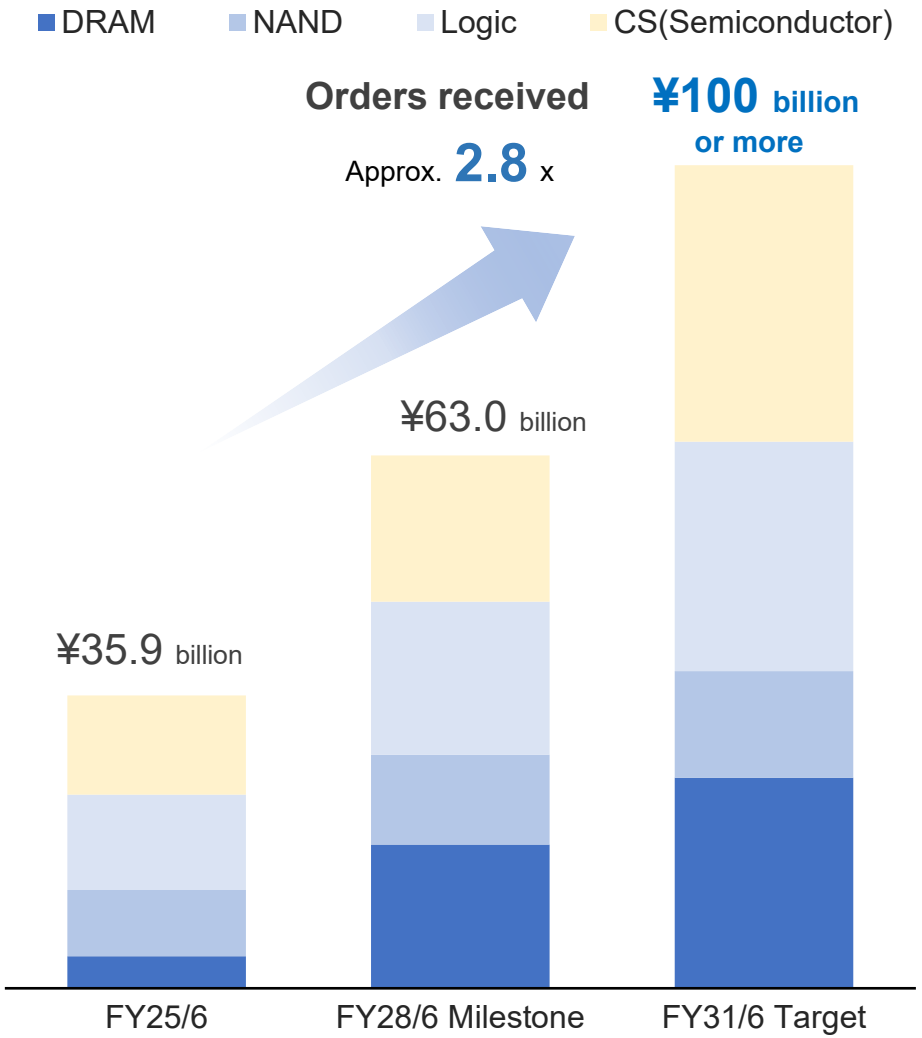
Growth Strategy : Semiconductor Growth Scenario

» Based on proven hard mask technology and metal film deposition technology, we will increase the number of POR*s for important customers and expand our market share by acquiring new processes, aiming for orders of ¥100 billion or more in FY31/6.



Growth Strategy

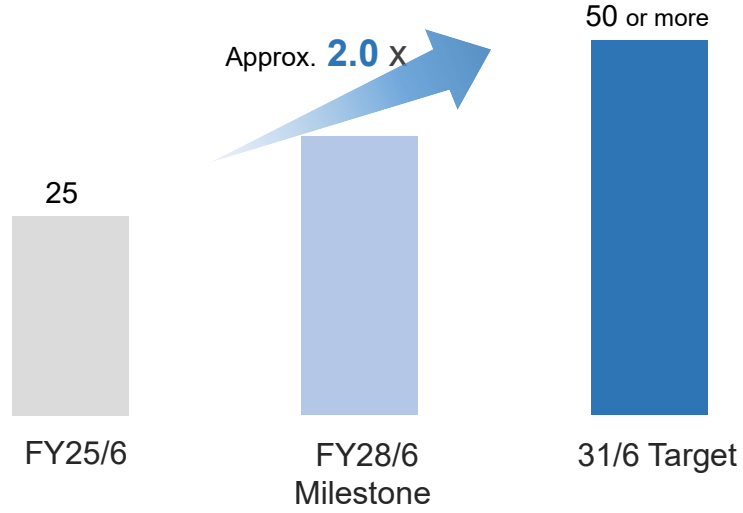
① Apply HM (Hard Mask) technology to high-density functional films.

② Establish a top position in HM processes and expand into Cu wiring applications.

③ Expand PVD market share by securing advanced logic Cu wiring and post-Cu wiring processes.

④ Expand and deepen the CS (Customer Support) business.

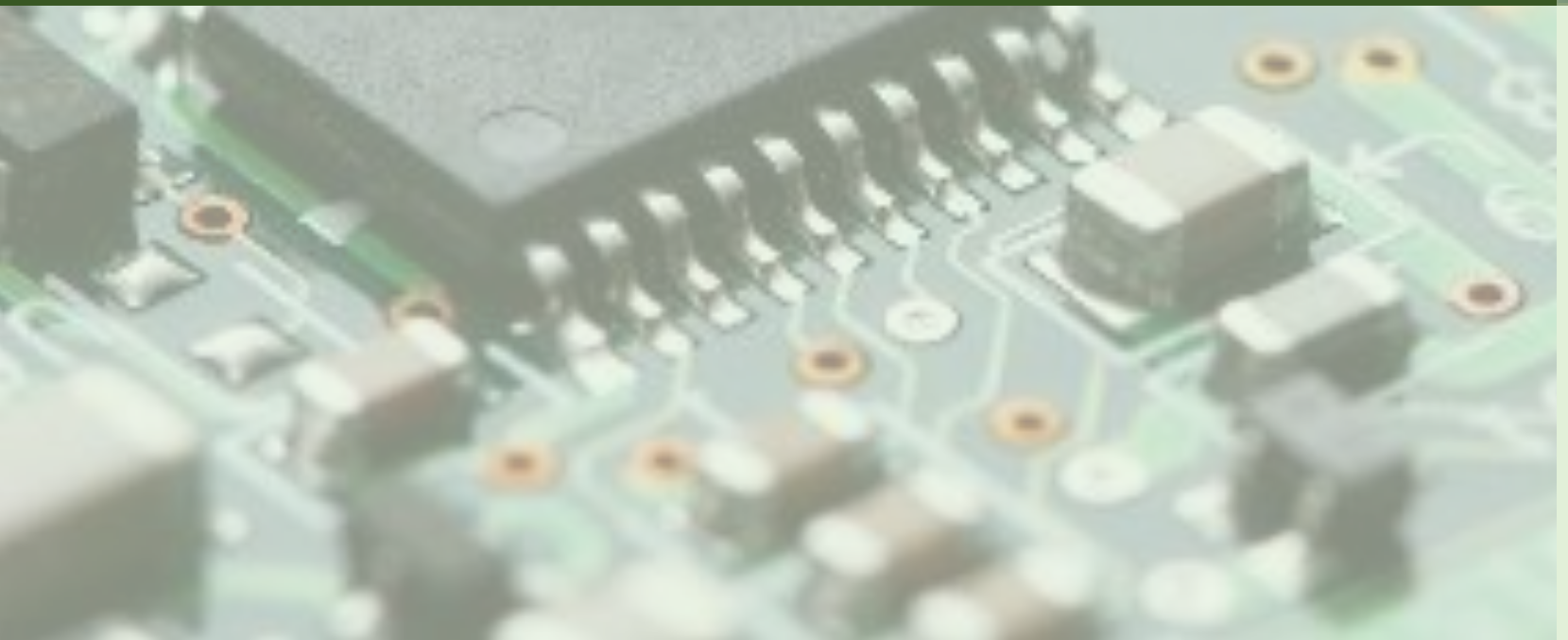
Number of important customers POR



* Process of Record: Certified process used in mass production

New Initiatives in Advanced Packaging

Harunori Iwai, Senior Executive Officer
Junya Kubo, Sales Department 2
Semiconductor and Advanced Electronics Business HQ



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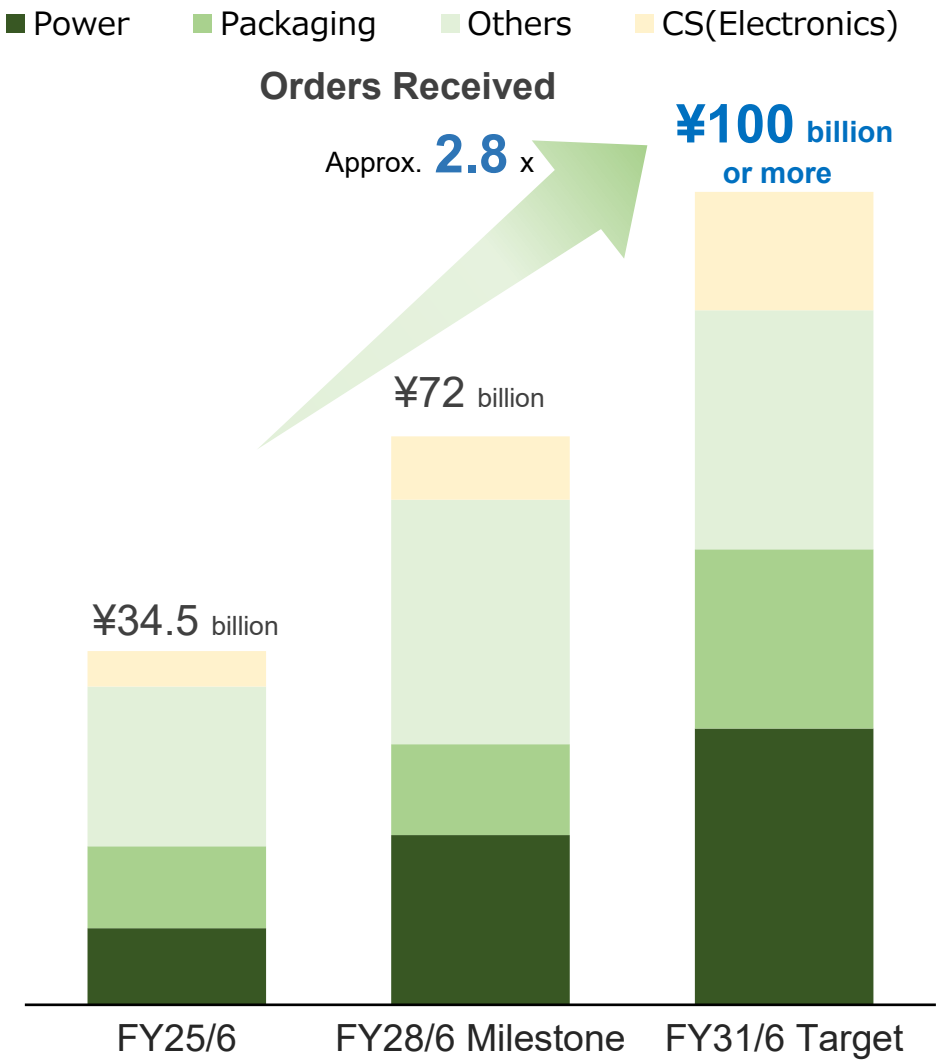
Growth Strategy: Growth Scenario for Electronic Devices

» We aim to expand to a business scale of over ¥100 billion and further growth mainly through the revitalization of the packaging business and the recovery of power device investments.



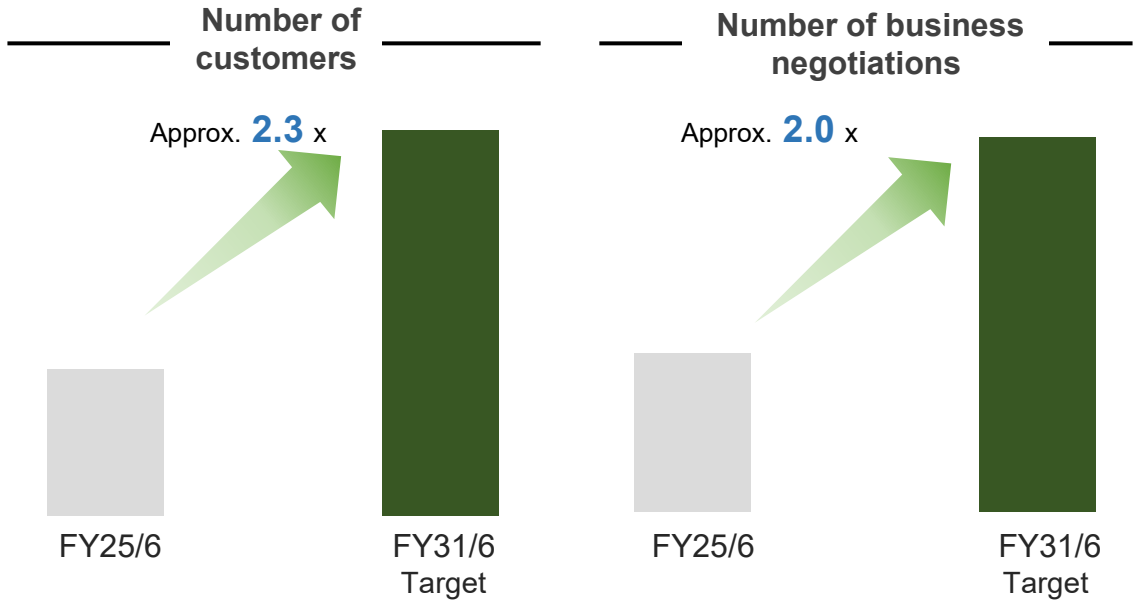
Growth Strategy

① Expand applications to support GaN mass production in addition to SiC sputtering and ion implantation.

② Capture new processes and benefit from increased investment in advanced packaging.

③ Develop optoelectronic fusion businesses through mass production of TFLN (Thin Film Lithium Niobate) etching, contributing to the miniaturization of communication devices.

④ Expand and deepen the CS business.



1. **Advanced Packaging**

2. **Surface Treatment Technologies used in Advanced Packaging**

Essential Elements for Packaging Required in AI Semiconductors

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- Speed
- Cooling Capacity
- Durability
- Mass productivity

The Role and Technological Evolution of Advanced Packaging

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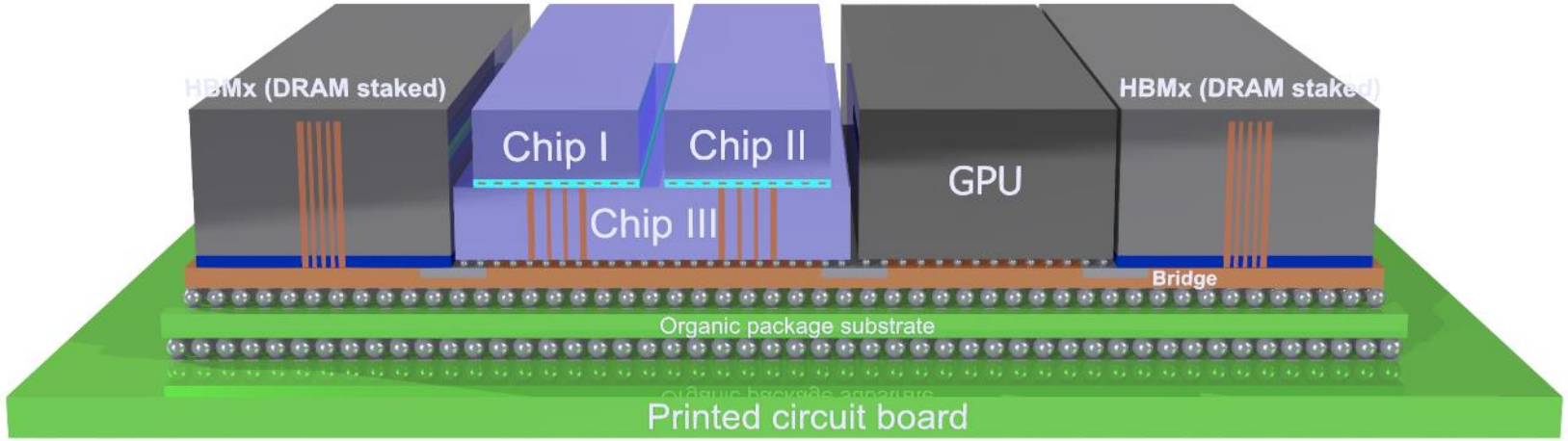
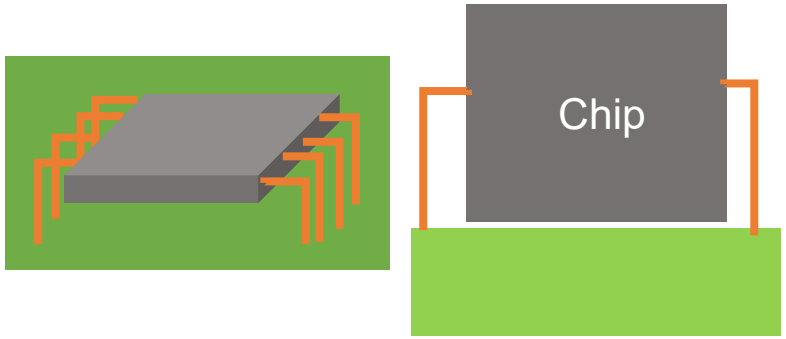
The Role of Packaging (Fine, Short, High-Density Wiring Connections)



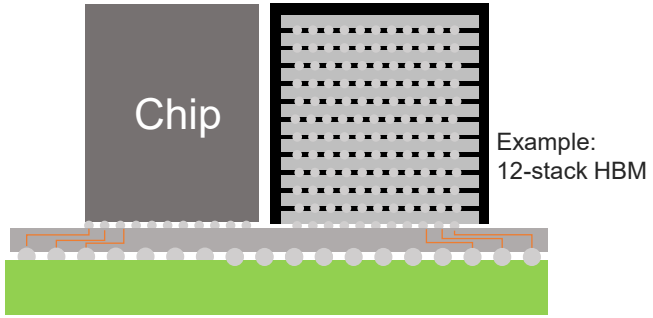
Evolution of 2D/3D PackagingTechnologies

Conventional Method | **Advanced Packaging 2.X D 3D**

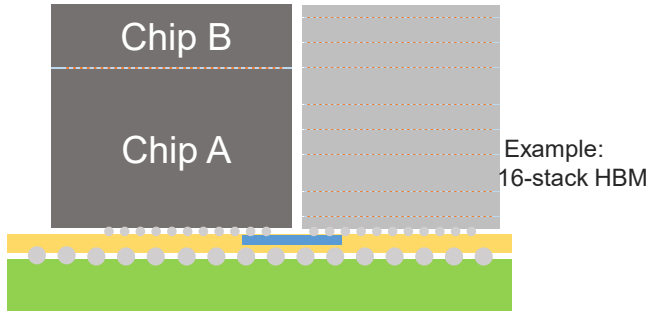
Wire Connection



Solder Bump Connection



Hybrid Bonding



Our Technologies Utilized in Advanced Semiconductor Packaging

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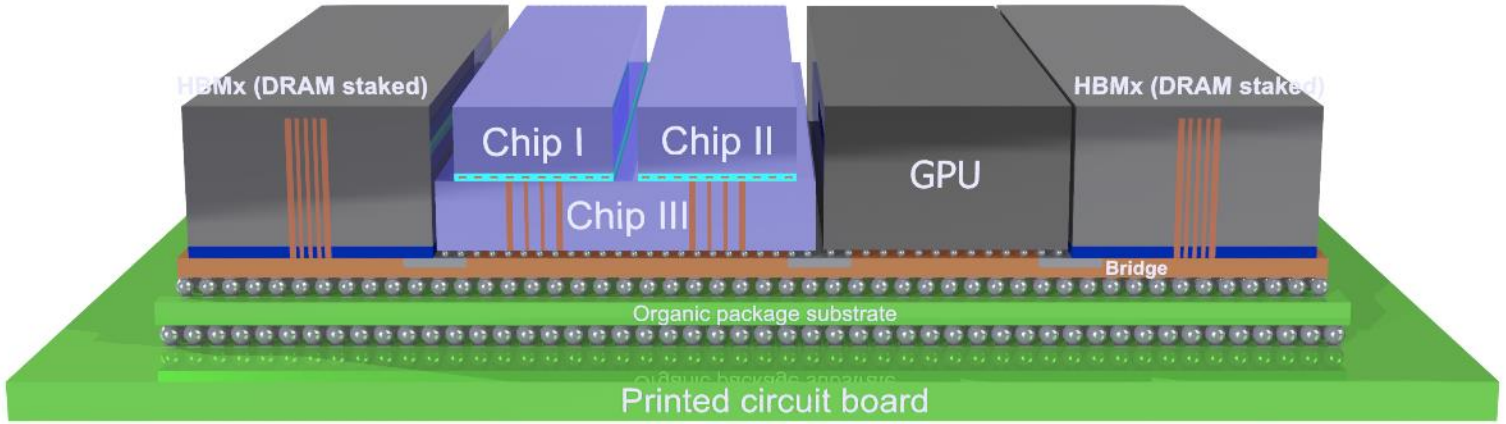
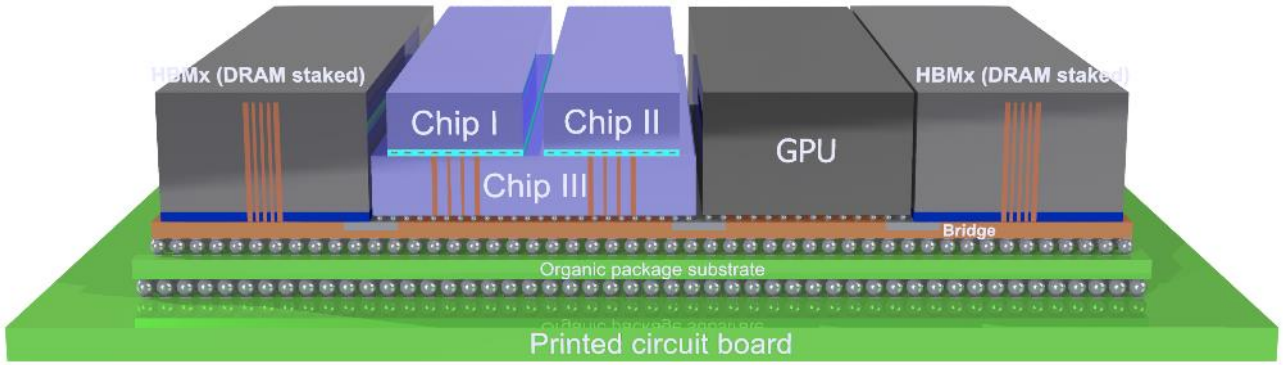


- Desmear Processing for Interposers
- Desmear processing for packaging substrates
- Etching for glass processing (optical waveguide formation)
- TGV Glass substrate patterning
- TSV Etching
- **Plasma surface activation (hybrid bonding)**
- Electrode formation sputtering
- Seed sputtering for packaging substrates
- Etching for fine patterning
- Plasma Dicing
- **Surface cleaning/hydrophilic treatment**

1. Advanced Packaging

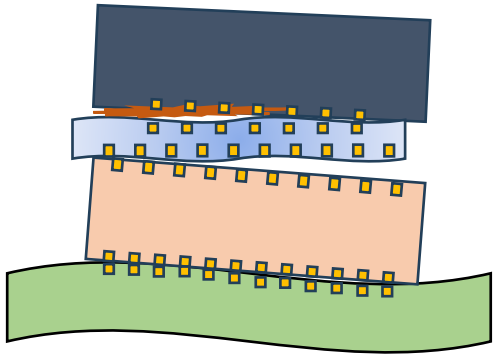
2. Surface Treatment Technologies used in Advanced Packaging

Key Points for Multilayer Structures in Advanced Packaging



Poor Connection

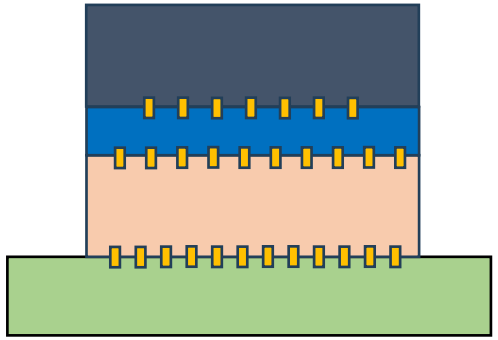
Distorted and dirty



Vs.

Good Connection

Clean and flat



Key Points for Multilayer Packaging

- Flat Surface
- Clean and good adhesion
- No degradation
- Efficient transfer of heat and electricity

Trends in Connection Technology

3 Methods for Connecting Semiconductors: Smaller, Denser, Thinner

Bump

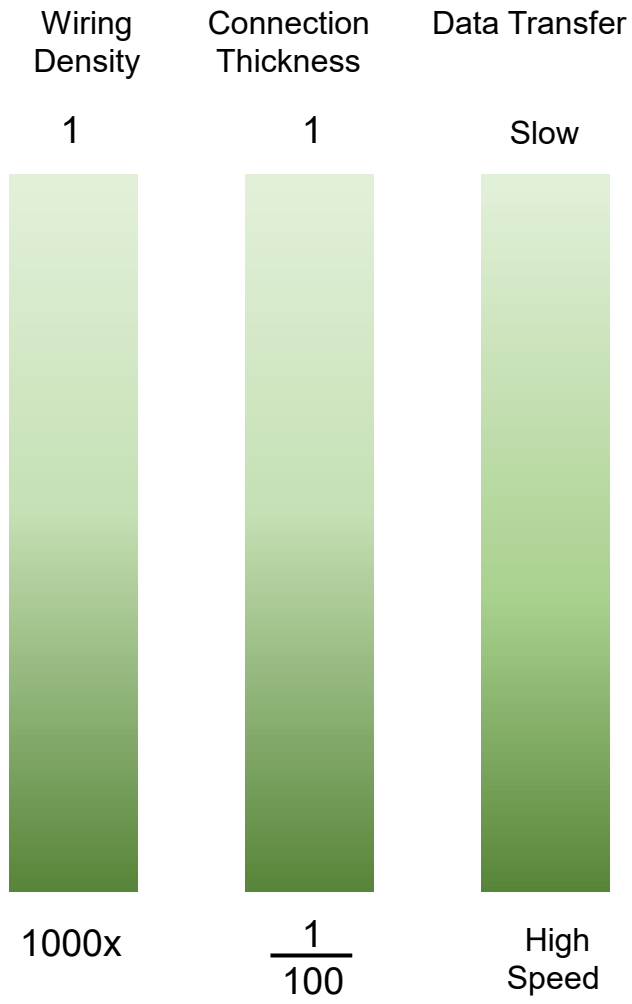
(Application Example) Board Interconnects, High-Current Applications

Micro Bump

(Application Example) HBM Stacked Memory

Hybrid Bonding

(Application Example) Next-generation HBM, Advanced 3D-IC



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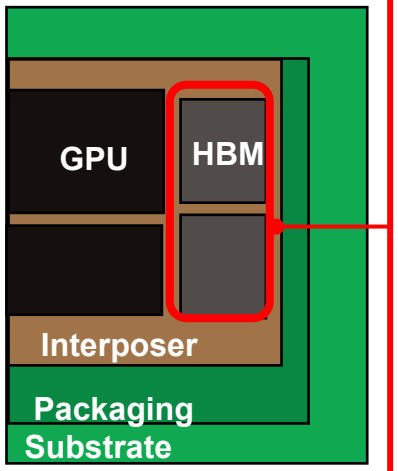
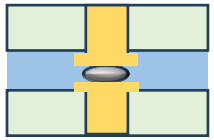
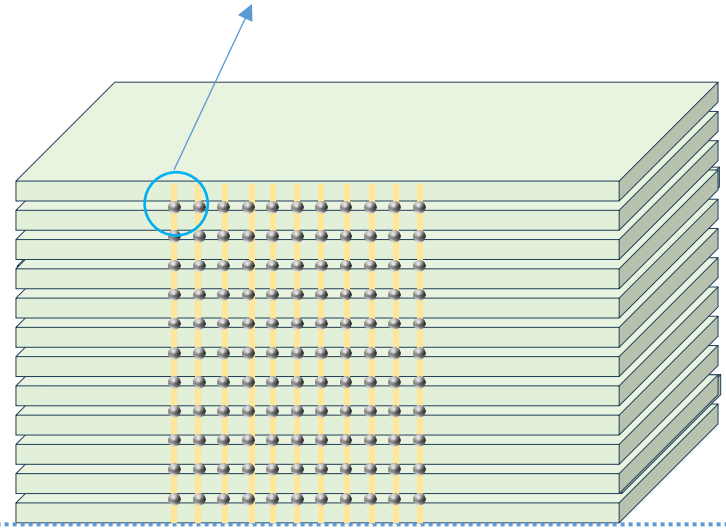
Evolution of Connection Methods in HBM



I. Microbump connection

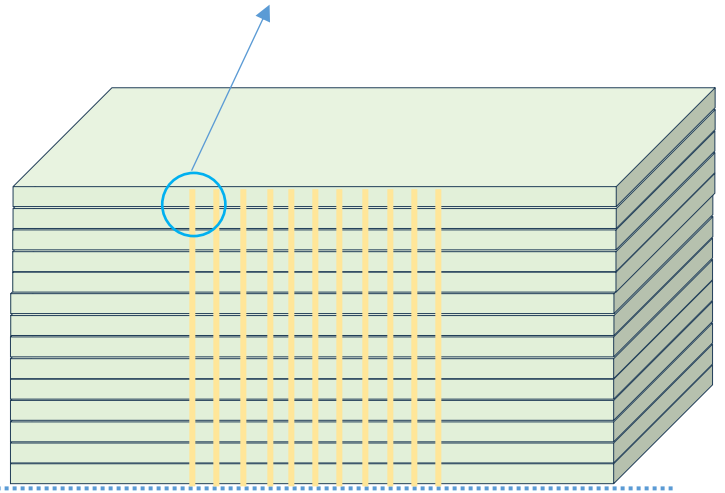


Connection thickness ≈ tens of μm



II. Hybrid bonding

Connection thickness ≈ several μm or less



Surface treatment technologies used in bump connections

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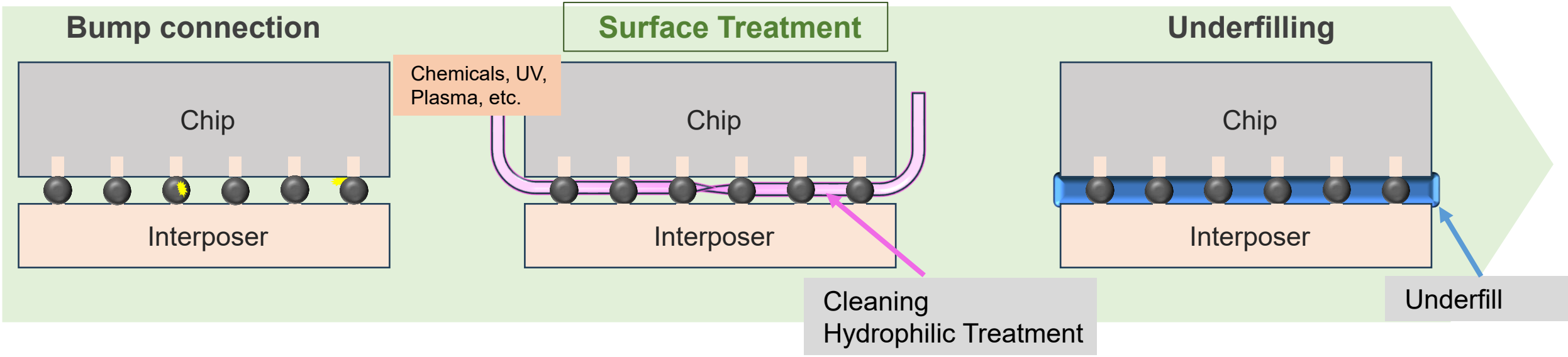
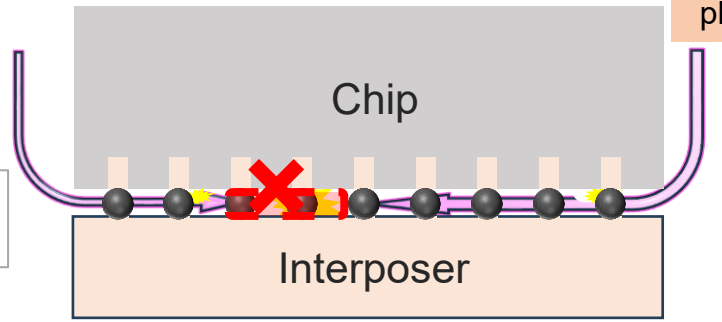
Surface treatment to stabilize bump connections



As chip and substrate gaps narrow and sizes increase in the future,

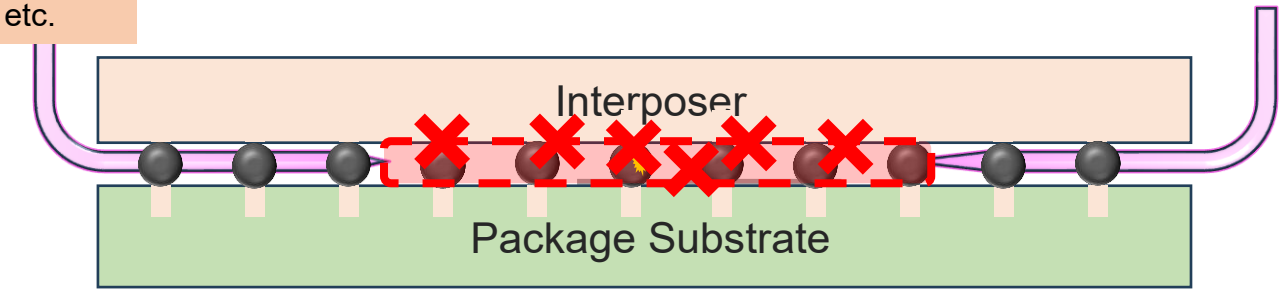
Challenges

× Uneven processing occurs



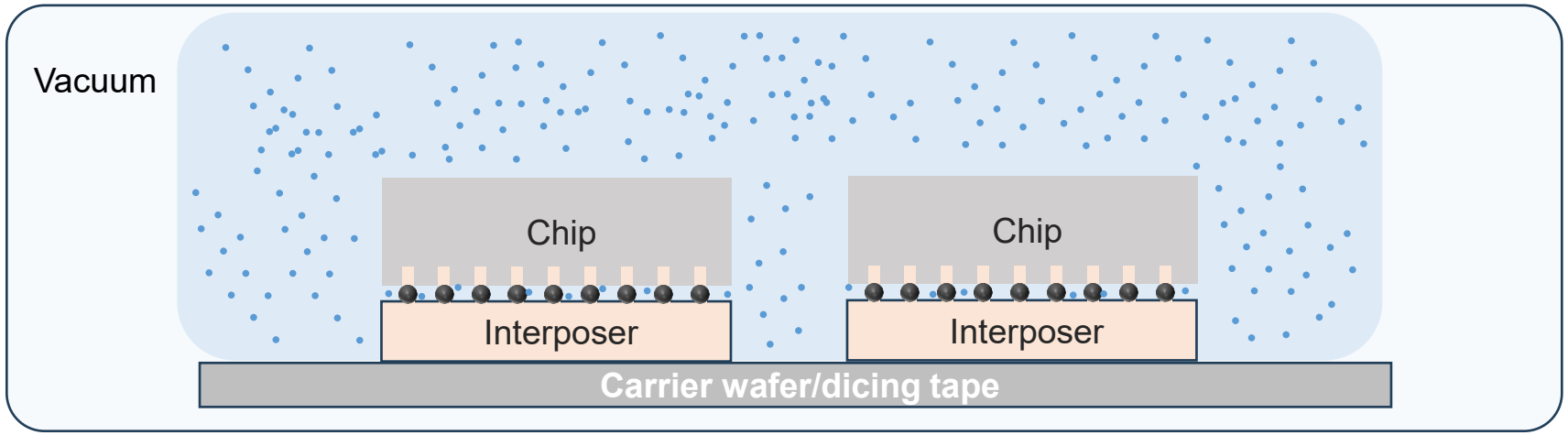
Chemicals, UV,
plasma, etc.

× Processing may not reach inside



Surface Treatment Technology Used in Bump Connections

Our Process: Vacuum + Radicals



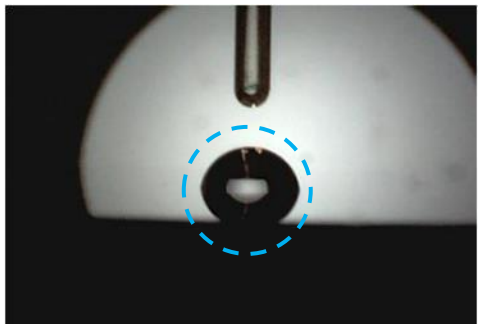
Our Process Equipment

Radical: Immediately disappear by highly reactive collide

Vacuum: Maintains radical effectiveness by prevents unnecessary collisions.

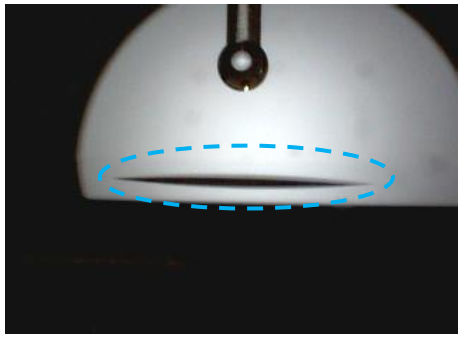
What is hydrophilic treatment?

Before



Making the surface water-repellent

After

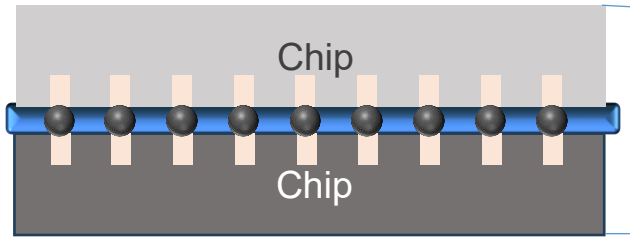


to a state where water adheres

Connection Technology: Hybrid Bonding

Hybrid Bonding Applications and Challenges

I. Microbump Connection

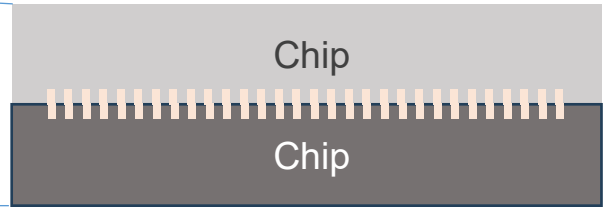


Advantages

- Increased wiring density
- Thinner due to bump thickness

Expected for application in high-performance semiconductors

II. Hybrid Bonding



Challenges

- High-precision surface treatment and alignment required
- Process optimization for mass production is a challenge

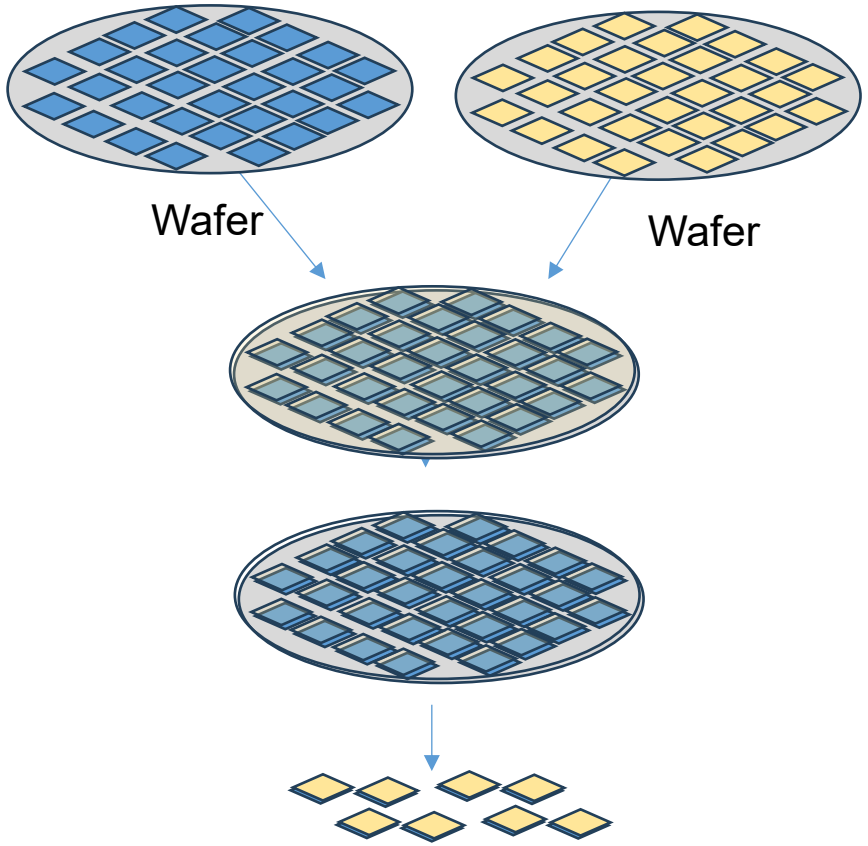
Expectations for process optimization toward mass production

Equipment optimization and mass production verification are required for packaging applications

Activation technology used in hybrid bonding

Types of hybrid bonding

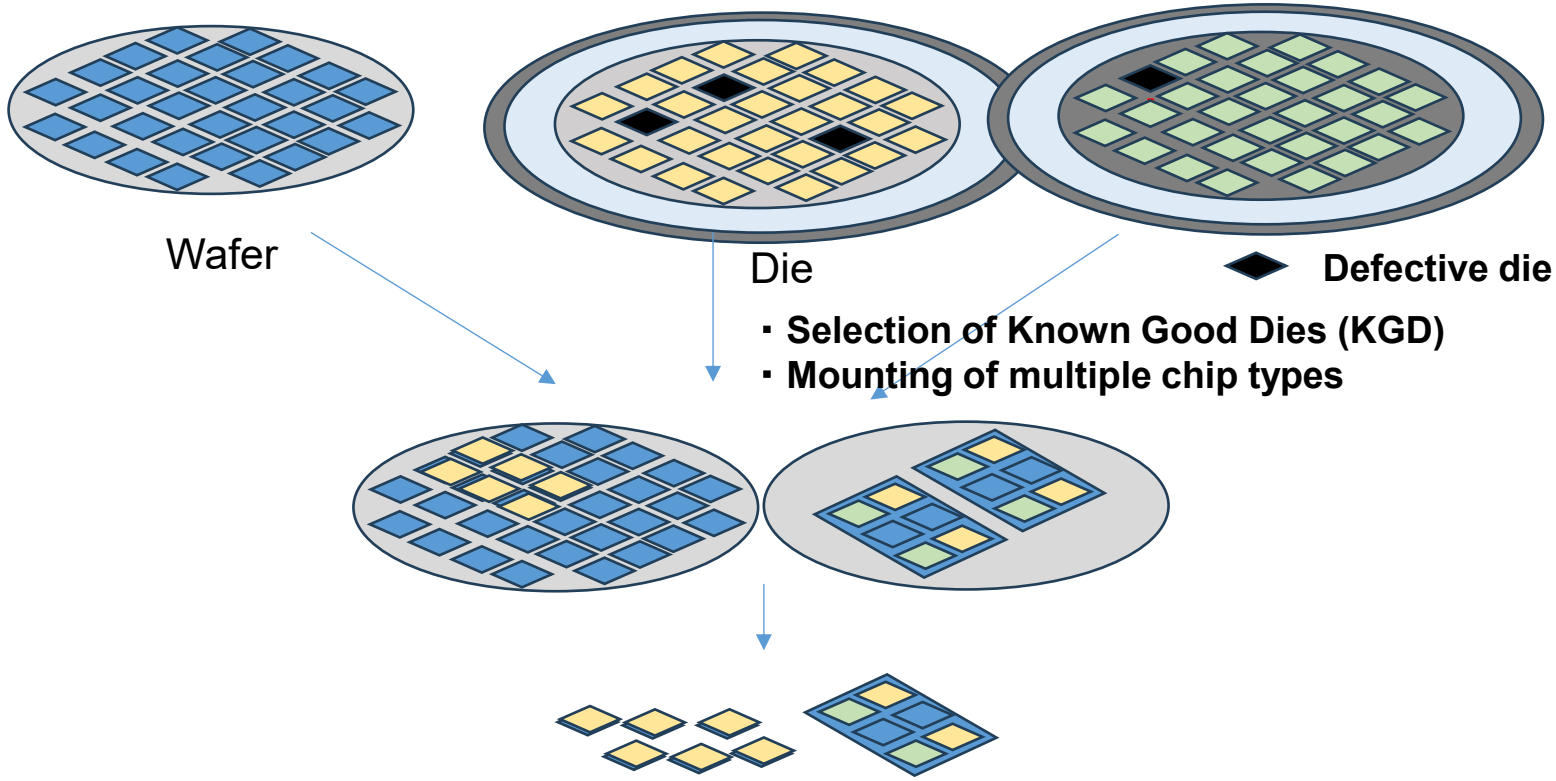
W to W (Wafer to Wafer)



Capable of attaching many chips at high speed
Mature and still evolving

D 2 W (Die to Wafer)

Our Focus

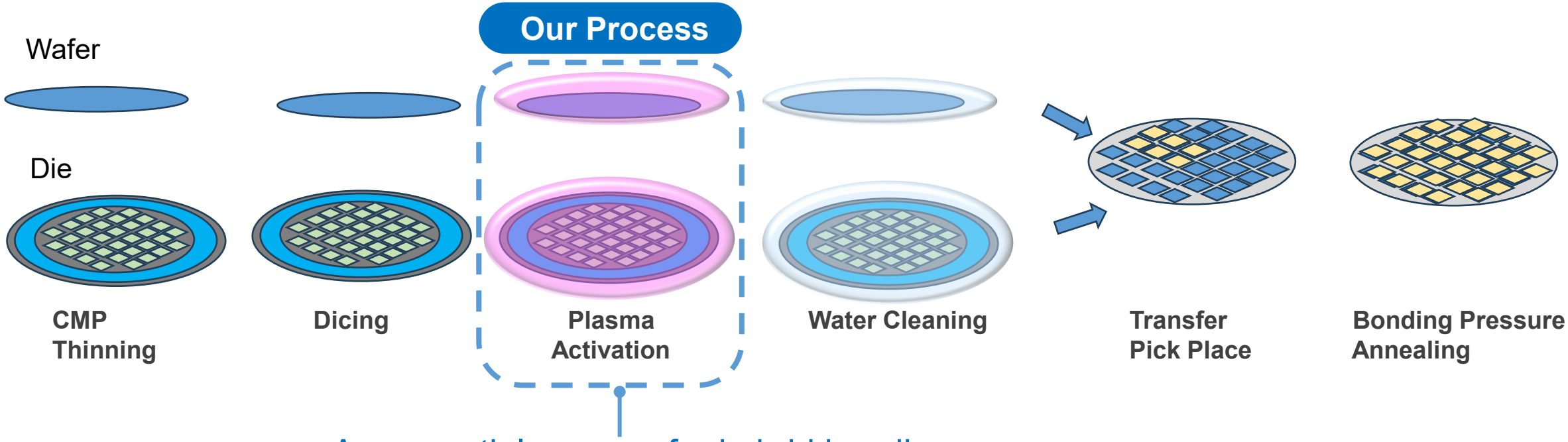


Good chip sorting and heterogeneous chip combination possible
Mass production development is progressing

Activation technology used in hybrid bonding

ULVAC

D2W Bonding



An essential process for hybrid bonding

Our Strength

- Improve substrate surface reaction with using gentle plasma
- Dedicated equipment capable of uniformly processing individual chips

Surface Treatment for Advanced Packaging and the Role of Our Equipment

ULVAC

Our Advantage for Bump Connection	Our Advantage for Hybrid Bonding
Smaller Scale	D2W
Hydrophilicity	Activation
Dicing Frame Compatibility	Dicing Frame Compatibility
Radical Treatment	Plasma Control

Roles of ULVAC

Optimal Surface Treatment × Stable Equipment Supply

Strengths and Future Development of Surface Analysis System

Hirohisa Takahashi
Executive Officer, President and Representative Director, ULVAC-PHI, Inc.
Takuya Miyayama
Senior Manager, Product Strategy Department, ULVAC-PHI, Inc.

ULVAC-PHI, INC.

ULVAC-PHI Corporate Profile Video

PHI Gr.

- **AES** Auger Electron Spectroscopy, **XPS** X-ray Photoelectron Spectroscopy, **SIMS** Secondary Ion Mass Spectrometry (TOF-SIMS, Q-pole-SIMS)
  The world's only company possessing all three surface analysis techniques (Hardware, Software)
- A leading surface analysis instrument manufacturer with **a strong track record of actual deliveries to national research institutes and top global companies** (over 2,000 units delivered, over 1,300 units in operation)
- ULVAC-PHI will leverage its XPS technology cultivated through surface analysis instruments for research and development to challenge the commercialization of XPS inspection equipment for semiconductor mass production lines by FY27/6, aiming to become a world-leading company in both analytical instruments and inspection equipment.

Auger electron spectroscopy (AES)

PHI 710

X-ray photoelectron spectroscopy (XPS)

PHI GENESIS

Secondary ion mass spectrometry (TOF-SIMS)

PHI nanoTOF 3+

Secondary ion mass spectrometry (Q-pole-SIMS)

PHI ADEPT1010

History

Founder
Dr. R. E. Weber
University of Minnesota

May,1969

PHYSICAL ELECTRONICS (PHI) founded by Dr. R. E. Weber of the University of Minnesota

- Developed the world's first commercial AES surface analysis instrument Subsequently added XPS and SIMS to its product lineup, establishing its position as a surface analysis supplier

April,1971

Nippon Vacuum Technology Co., Ltd. (now ULVAC, Inc.) signed an exclusive agency agreement with PHI

November,1982

PHI and Nippon Vacuum Technology Co., Ltd. established the joint venture ULVAC-PHI Co., Ltd.

February,2003

Acquired the Surface Analysis System business division from PHI and commenced manufacturing and global sales of surface analysis instruments

November,2023

Established a new company, ULVAC PHI Instruments, in China

Present

Operating globally through three companies: ULVAC-PHI (Japan), PHYSICAL ELECTRONICS (U.S.), and ULVAC PHI Instruments (China)

Value Proposition

Through analytical technologies that "convert the invisible into data and information“, we provide critical data and information that supports customers’ decision-making.

Strengths

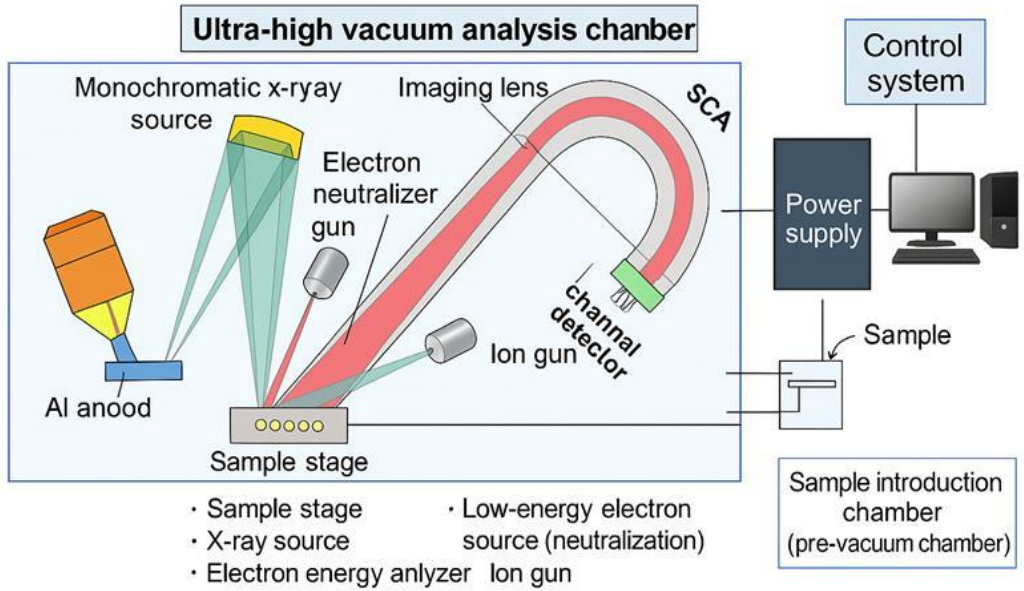
① Technology featuring high-precision, wide-ranging surface analysis techniques

	Surface analysis methods of competitors		ULVAC	A	B	C	D	E
Analysis Method	**XPS** X-ray Photoelectron Spectroscopy		●	●	●	●		
	AES Auger electron spectroscopy		●			●		
	SIMS Secondary Ion Mass Spectrometry	**TOF-SIMS** Top Surface Analysis	●				●	
		D-SIMS Depth Analysis	●					●

Excerpt from FY24.6 Q4 Financial Results Disclosure Materials

② Total coordination of analytical instruments

- Hardware: Challenging detection limits
- Software : Converting signals into data and information
- System: Integrated Value Chain

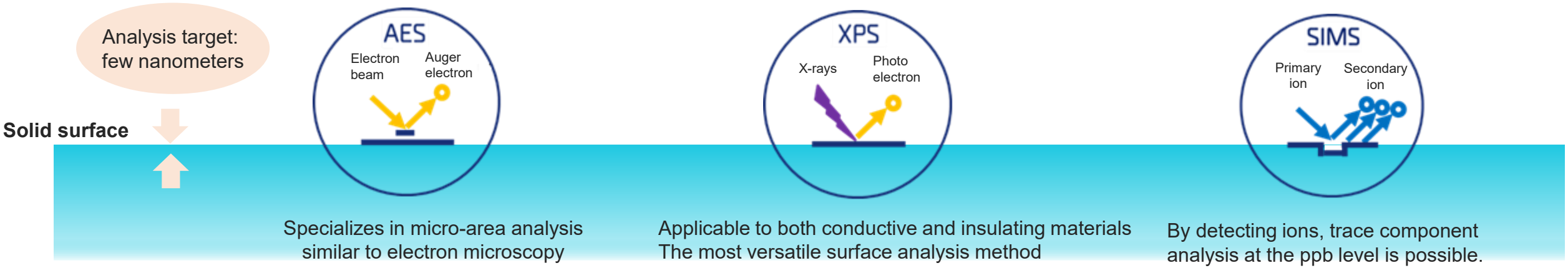


Standard XPS system configuration

Core Technology: What is Surface Analysis

- Analysis of elemental composition, chemical states, and molecular structure in the surface region at the nanometer scale
- A technique that enables material evaluation by combining two-dimensional distribution observation (imaging) and depth profiling analysis.

	AES (Auger electron spectroscopy)	XPS（X-ray photoelectron spectroscopy）	SIMS（Secondary ion mass spectrometry）
Excitation source	Electron beam（e^-）	X-rays (Al Kα radiation,etc.)	Primary ion beam (Cs, O2, Bi, etc.)
Detected signal	Auger electron	Photoelectron	Secondary ion
Measurement content example	Evaluation of contamination on fine wiring, etc.	Evaluation of thin film composition film thickness, etc.	Analysis of low-concentration elements, etc.

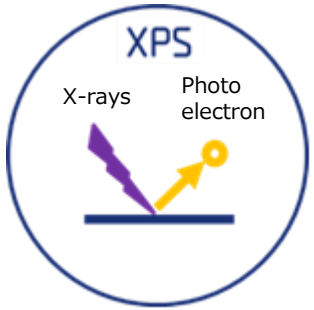


Specializes in micro-area analysis similar to electron microscopy

Applicable to both conductive and insulating materials
The most versatile surface analysis method

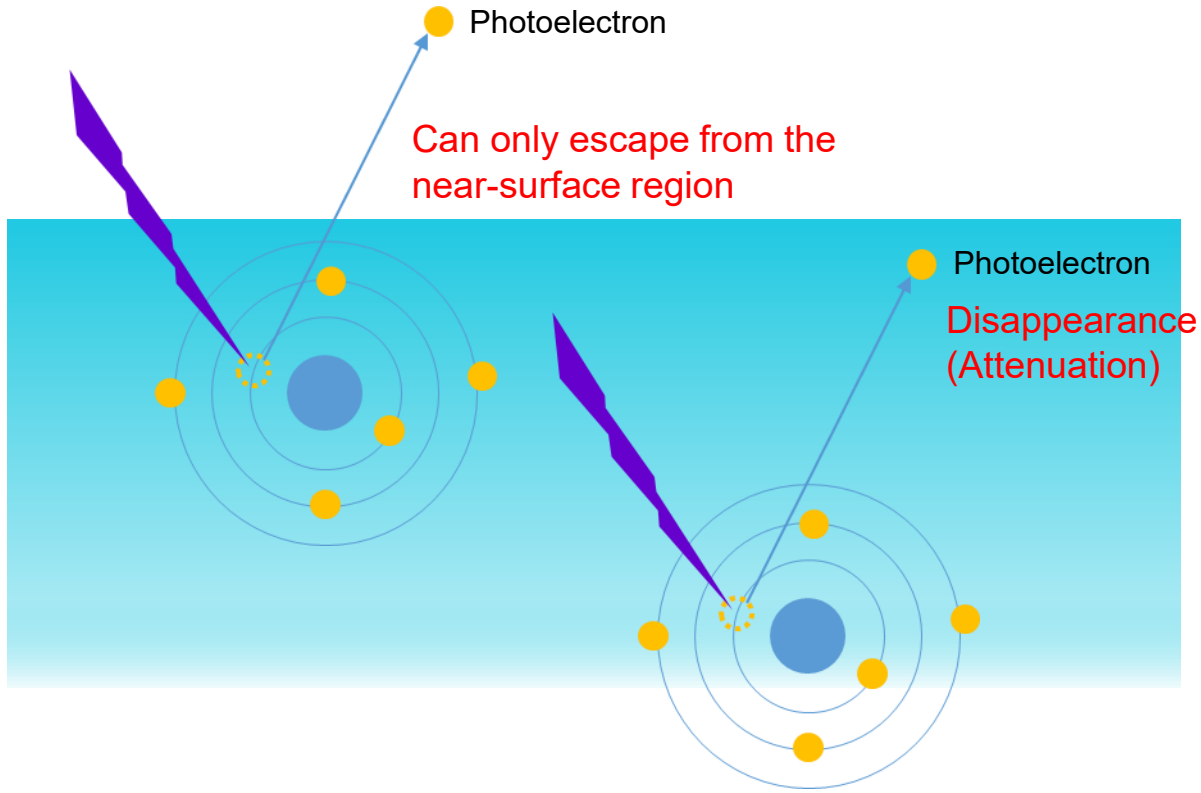
By detecting ions, trace component analysis at the ppb level is possible.

Core Technology: Surface Analysis Technology



XPS (X-ray Photoelectron Spectroscopy)

An analytical method that utilizes the photoelectric effect, in which electrons are emitted from a material when it is irradiated with X-rays.



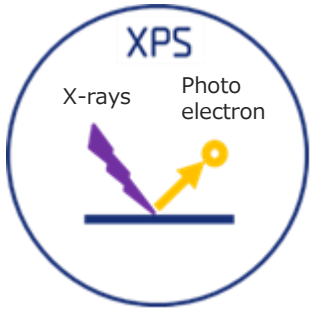
The reason why XPS is a surface-sensitive technique

- Electrons lose energy and attenuate within the material.
- The distance electrons can travel within the material is at most a few nanometers.

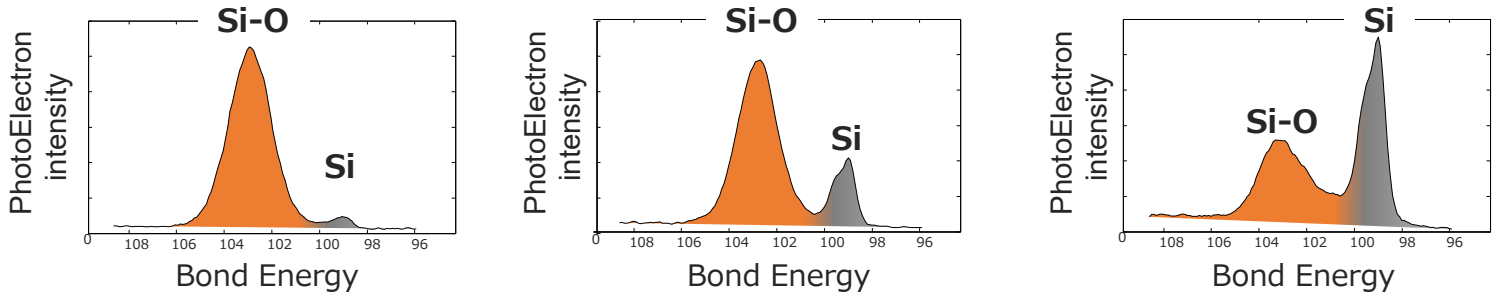
Technologies Required for XPS

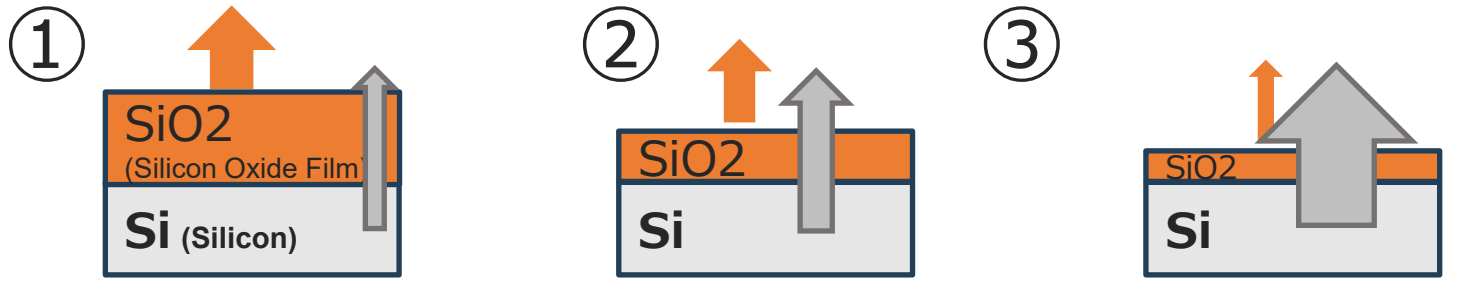
- X-ray Source
- Photoelectron Analyzer
- Ultra-High Vacuum (Ulvac's Core Technology)

Benefits of surface analysis: thin film thickness measurement



Si2p spectrum



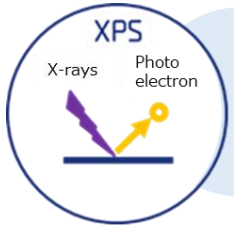


	①	②	③
SiO2 film thickness	Thick (Approx.10nm)	→	Thin (less than 1 nm)
Signal intensity from Si substrate	Weak	→	Strong

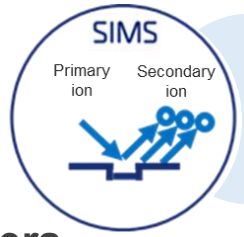
Thickness evaluation possible for thin films below 10 nm

Surface analysis techniques: essential technologies for semiconductor evaluation

Transistor (FEOL)

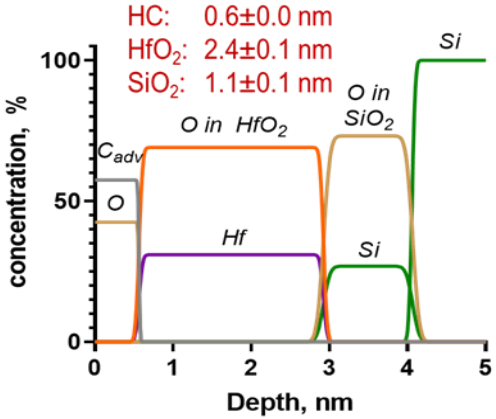


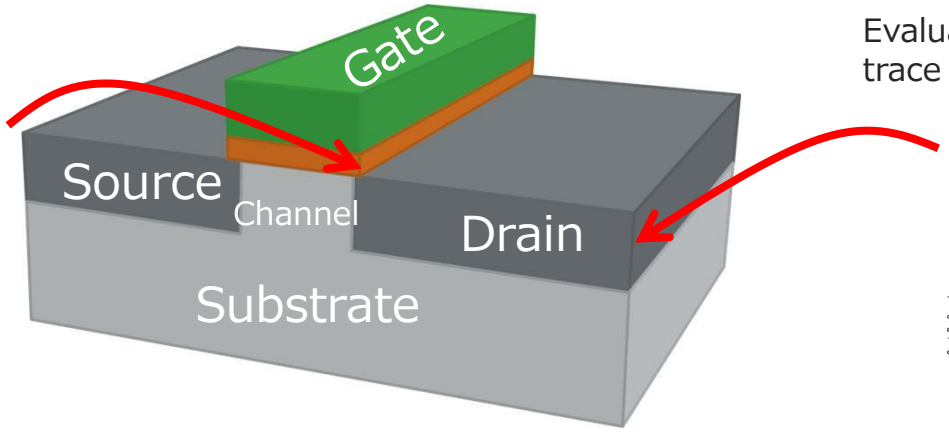
XPS
Non-destructive compositional evaluation of gate oxide film thickness



SIMS
Ion Implanter evaluation for source/drain formation

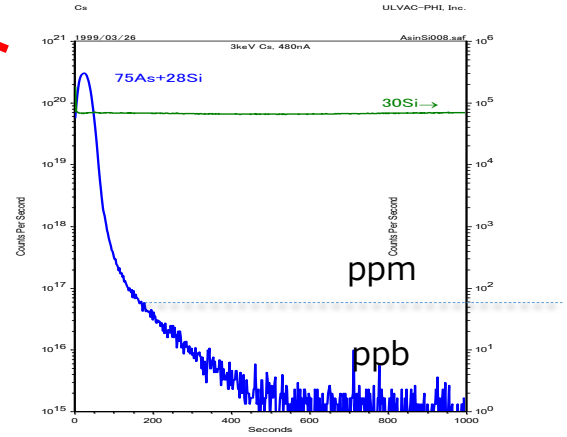
✓ **Film thickness evaluation of a few nanometers**



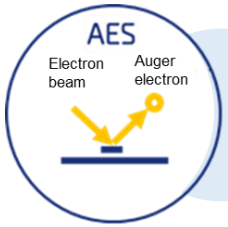


✓ **ppb-level dopant evaluation**

Evaluation and measurement of extremely trace amounts of dopants (impurity elements)

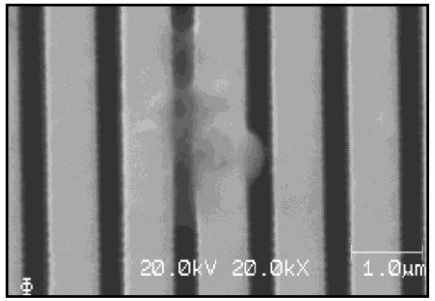


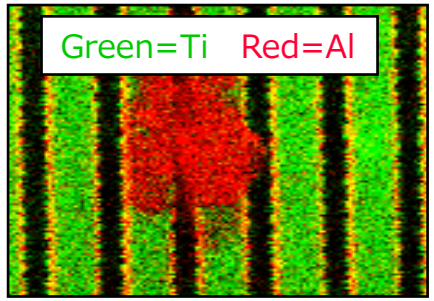
Wiring (BEOL)



AES
Contamination/foreign matter evaluation of the trench area

- ✓ Micro-area analysis similar to electron microscope observation
- ✓ Evaluation of contamination/foreign substances on the extreme surface layer





Application Fields of Surface Analysis Technology

ULVAC-PHI, INC.

PHYSICAL ELECTRONICS

Fuel Cell

Mineral

Semiconductors

Glass

Polymer

Catalyst

Perovskite

Biotechnology

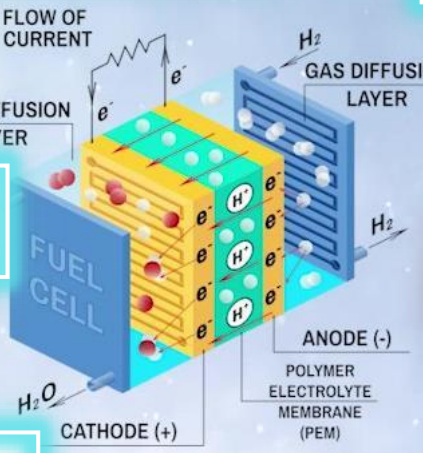
Pharmaceutical

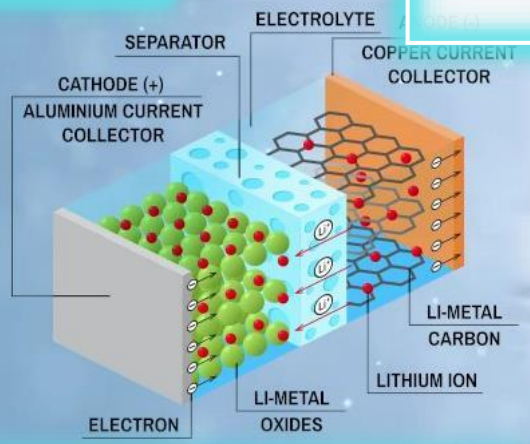
Solar cells

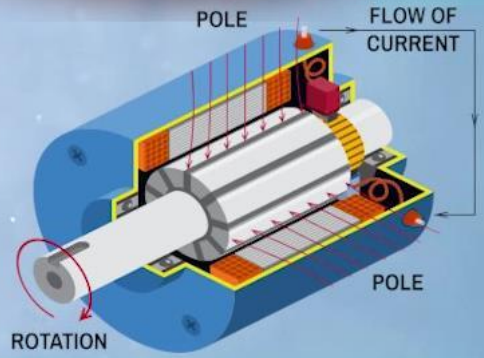
Lithium-ion batteries

Metal

Display





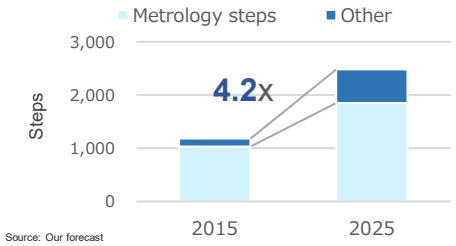


Challenge from Lab to Fab

» Leveraging experience and achievements in the existing Lab-type model (market share No. 1), we aim to establish a global position in the inspection equipment market by fully introducing "XPS" into the Fab-type model, where the importance of analysis increases due to the advancement of manufacturing processes, through synergies between semiconductors and electronics and other

Market Environment

The semiconductor manufacturing process has doubled in the past 10 years, with the inspection process increasing fourfold.



Technology and Market Trends

- Increase in process steps due to advances in miniaturization
- Growing demand for yield improvement
- Increased importance of quality control

Our Strengths

- Our track record as surface analysis specialist manufacturer
- R&D to service integrated system
- Providing value from both Software (Science) /Hardware (Physical and Optical Design,Manufacturing)

by FY25/6

Top share in XPS analysis equipment for research and development

- Expansion of XPS analysis equipment for research and development
- Prototype development of XPS inspection equipment for semiconductor mass production lines

XPS analysis equipment for research and development

by FY27/6

Market launch of XPS inspection equipment for semiconductor mass production lines

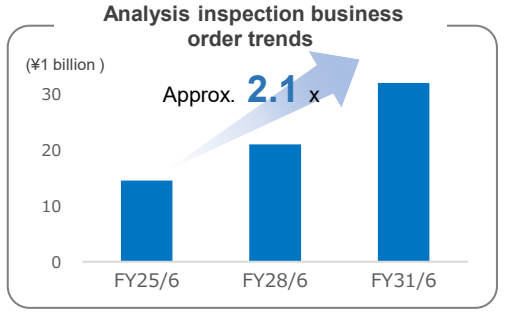
- Improvement of XPS analysis equipment for research and development
- **Product release of XPS inspection equipment for semiconductor mass production lines**

XPS inspection equipment for semiconductor production lines Image

by FY31/6

Aiming for further expansion through scaling global operation

- Expansion of the lineup of analytical instruments for research and development
- Expansion of production capacity for XPS inspection equipment for semiconductor mass production lines
- Commercialization of a business generating **¥30 billion** in orders for analytical instruments and inspection devices



Differences in Requirements Specifications for Analytical Instruments and Inspection Equipment

	Analytical Instruments	Testing Equipment
Takt Time	Not specified	Required
Measurement Target (Materials/Composition)	Unknown	Known
Measurement Method	Destructive	Non-destructive

Business Synergy Between Semiconductors and Electronics BU and ULVAC-PHI

We are aiming to realize XPS inspection equipment for semiconductor mass production lines by combining both companies' assets

ULVAC-PHI

Surface Analysis Technology (Hardware, Software)

ULVAC Semiconductors and Electronics Business Division

Mass production-level handling, low particle, takt time

Business Synergy

XPS Inspection Equipment for Semiconductor Mass Production Lines

Release in FY27/6

Aiming for commercialization of a ¥30 billion-scale business in analytical instruments and inspection equipment by FY31/6

Seamless provision of data and information from R&D (analytical instruments) to mass production (inspection equipment)
Solutions for production equipment and inspection equipment

ULVAC