ULVAC IR Seminar 2024

Expansion of Semiconductor Electronics Business Pioneered by Generative AI

Dec.9,2024

Today's Agenda

I. Logic and Memory Technology Trends and Our Approaches

Executive Officer, Semiconductor Marketing
Hiroaki Iwasawa

II. Current Status of Advanced Packaging and Our Approaches

Executive Officer, General Manager of Advanced Electronics Equipment Division
Harunori Iwai

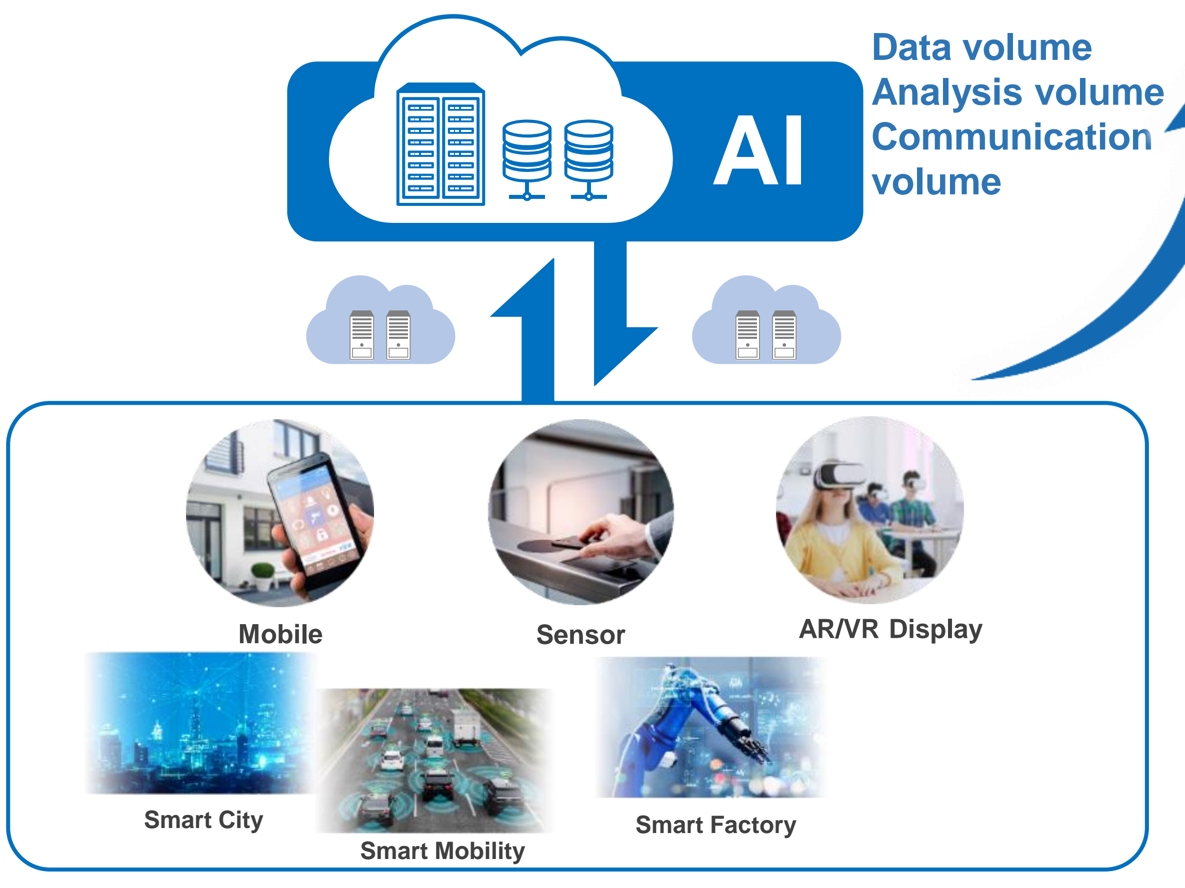
Assistant Manager, Business Planning Department,Advanced Electronics Equipment Division
Junya Kubo

Disclaimer regarding forward-looking statements etc.

- **Forward-looking statements**
  Forward-looking statements of the company in this presentation are based on information that was available at the time these documents were prepared. There are several factors that directly or indirectly impact the company performance, such as the global economy; market conditions for FPDs, semiconductor, electronic devices, and raw Materials; trends in capital expenditures and fluctuations in exchange rates. Please note that actual business results may differ significantly from these forecasts and future projections.
- **About this document**
  Please note that the IR seminar materials and explanations have not been prepared for technical purposes, and some parts have been simplified to facilitate investors' understanding. This document has been translated from the Japanese original for reference purpose only. In the event of any discrepancy between this translated document and the Japanese original, the original shall prevail.

Copyright© 2024, ULVAC, Inc. All rights reserved

AI Semiconductor



Power consumption is reduced to 1/20

Copyright© 2024, ULVAC, Inc. All rights reserved

What are AI Semiconductors?

Generated AI Market Demand Forecast (Global)

(Unit: $1 billion)

Source: Japan Electronics and Information Technology Industries Association

Copyright© 2024, ULVAC, Inc. All rights reserved

Elements required for AI semiconductors

Semiconductor miniaturization

Adoption to HBM

Application of new materials

Application of new structure

Copyright© 2024, ULVAC, Inc. All rights reserved

Approach to realize the elements required for AI semiconductors

Elements required for AI semiconductors

- Semiconductor miniaturization
- Adoption to HBM
- Application of new materials
- Application of new structure

Approach toward realization

- Maximizing PVD coverage
- Increasing in cutting-edge projects with development tailored to customer needs
- Utilizing FPD and other technologies

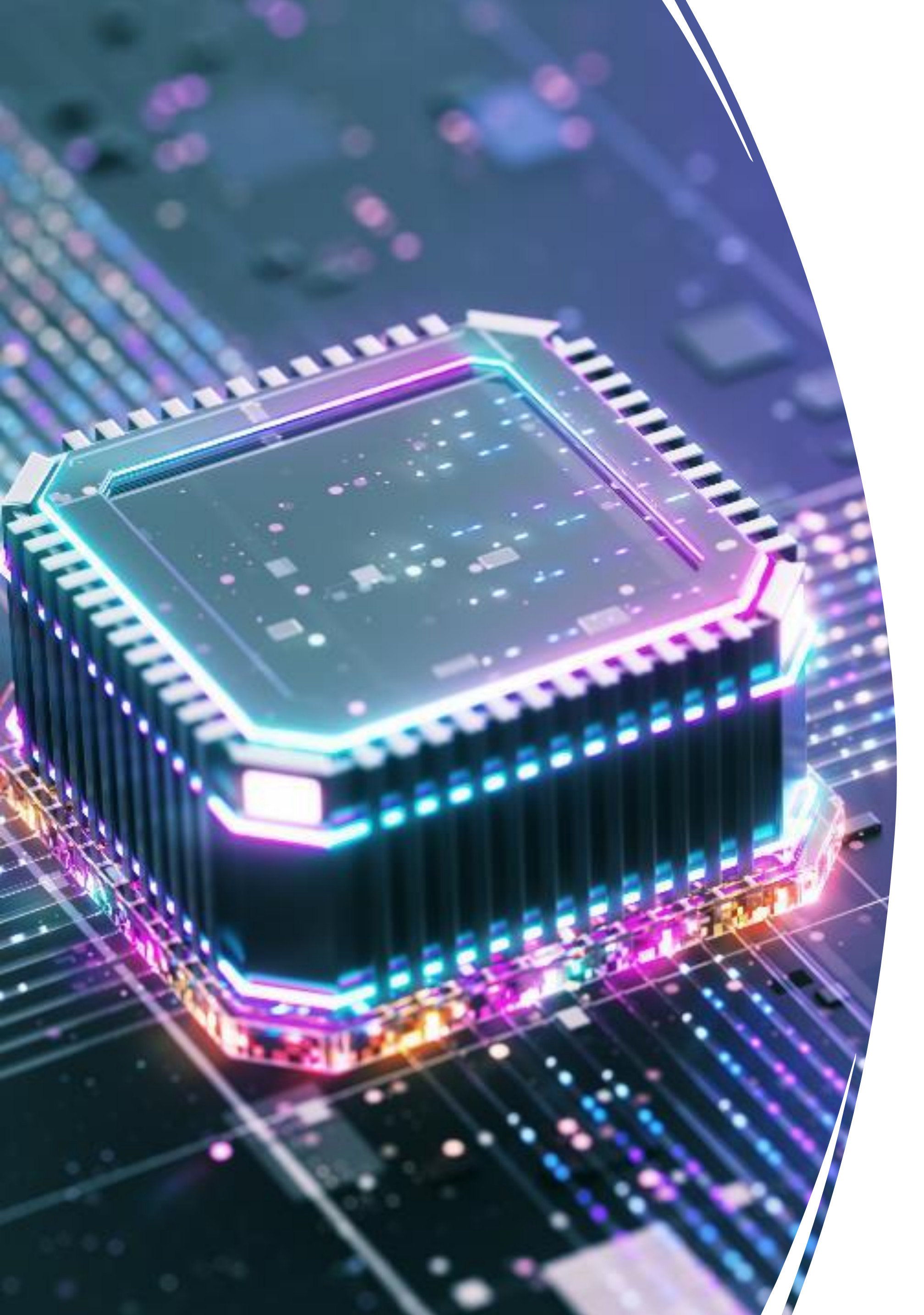
Expansion of our business opportunities

Copyright© 2024, ULVAC, Inc. All rights reserved

Expand growth of Semiconductor & Packaging business

Semiconductor & Packaging Long-Term Order Targets

Copyright© 2024, ULVAC, Inc. All rights reserved



Logic and Memory Technology Trends and Our Approach

Executive Officer, Semiconductor Marketing
Hiroaki Iwasawa

Elements required for AI semiconductors

Semiconductor miniaturization

Adoption to HBM

Application of new materials

Application of new structure

Copyright© 2024, ULVAC, Inc. All rights reserved

Semiconductor Business Progress in Logic Market

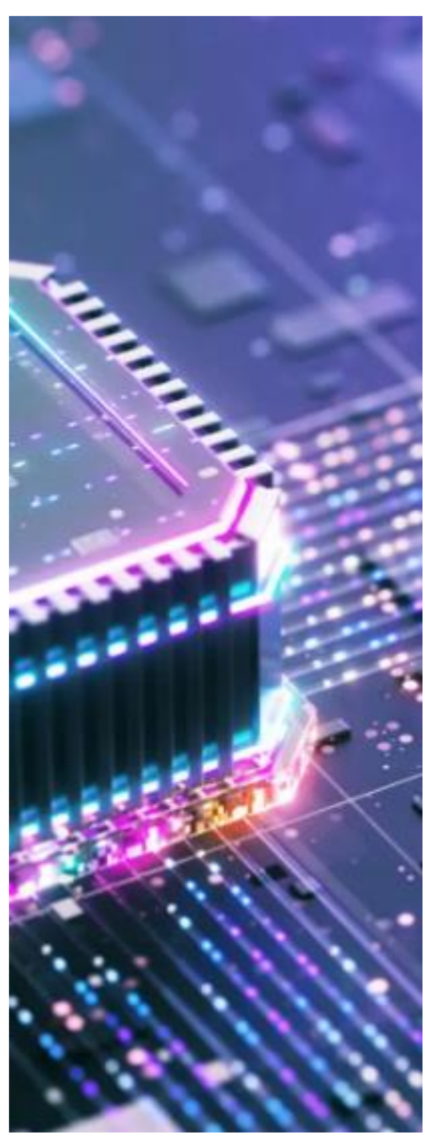
Order forecast (Unit: $ 1 billion)

Successful entry into the Logic market

- ✓ Expanding the number of customers
- ✓ From advanced EUV process to legacy product DUV process
- ✓ Expanding the adaptation of using a metal layer

Further growth due to increase in number of customers and processes

Copyright© 2024, ULVAC, Inc. All rights reserved

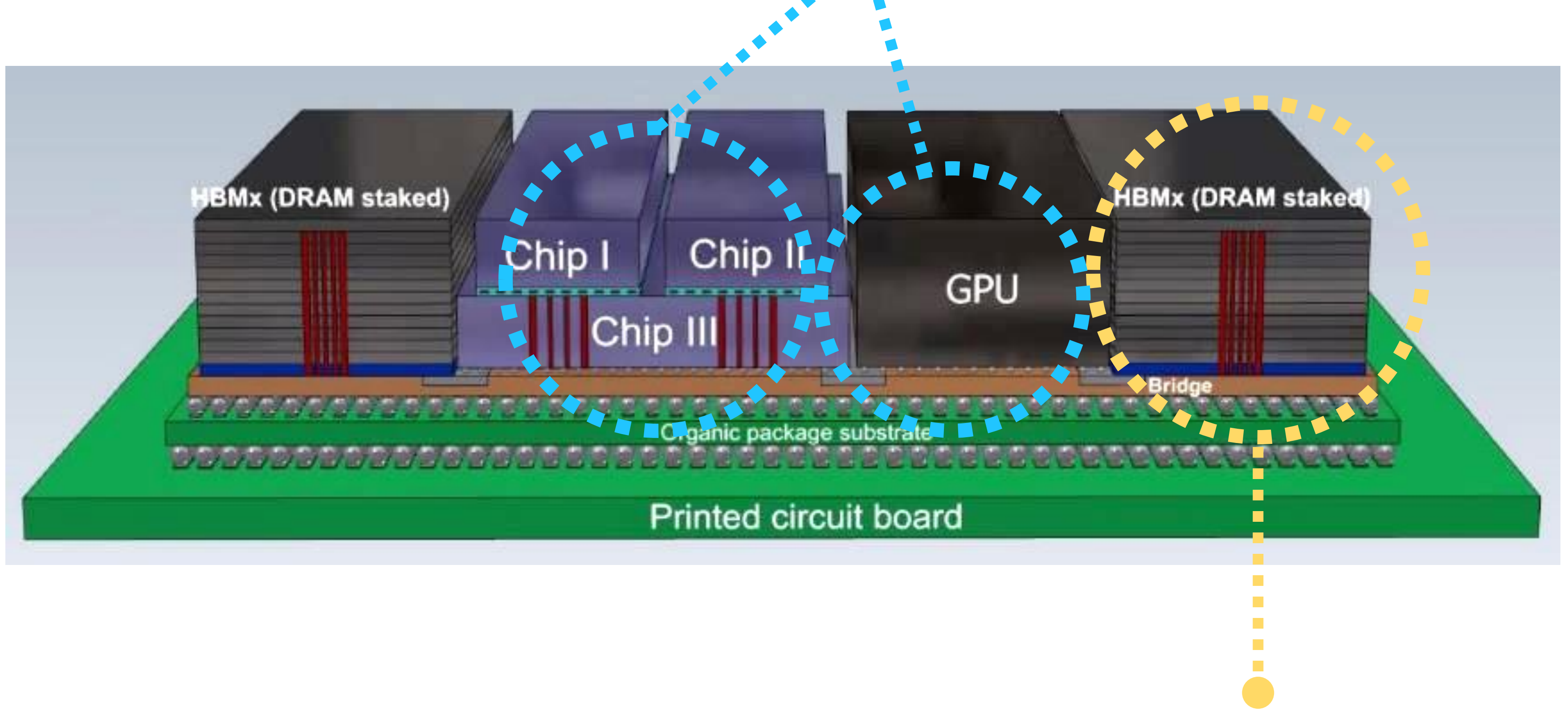


1. ULVAC PVD films and their strengths in a complex process
2. Our contribution in memory products for AI and adaptation of hardware
3. New Platform ENTRON-EXX

Copyright© 2024, ULVAC, Inc. All rights reserved

Advanced AI Chipsets:Semiconductor Products and Technologies Required ULVAC

1. Advanced Logic Products
   Our Contribution and Strengths of PVD Films



2. HBM (layered memory) for AI processors
   Our Contributions and Strengths

Copyright© 2024, ULVAC, Inc. All rights reserved

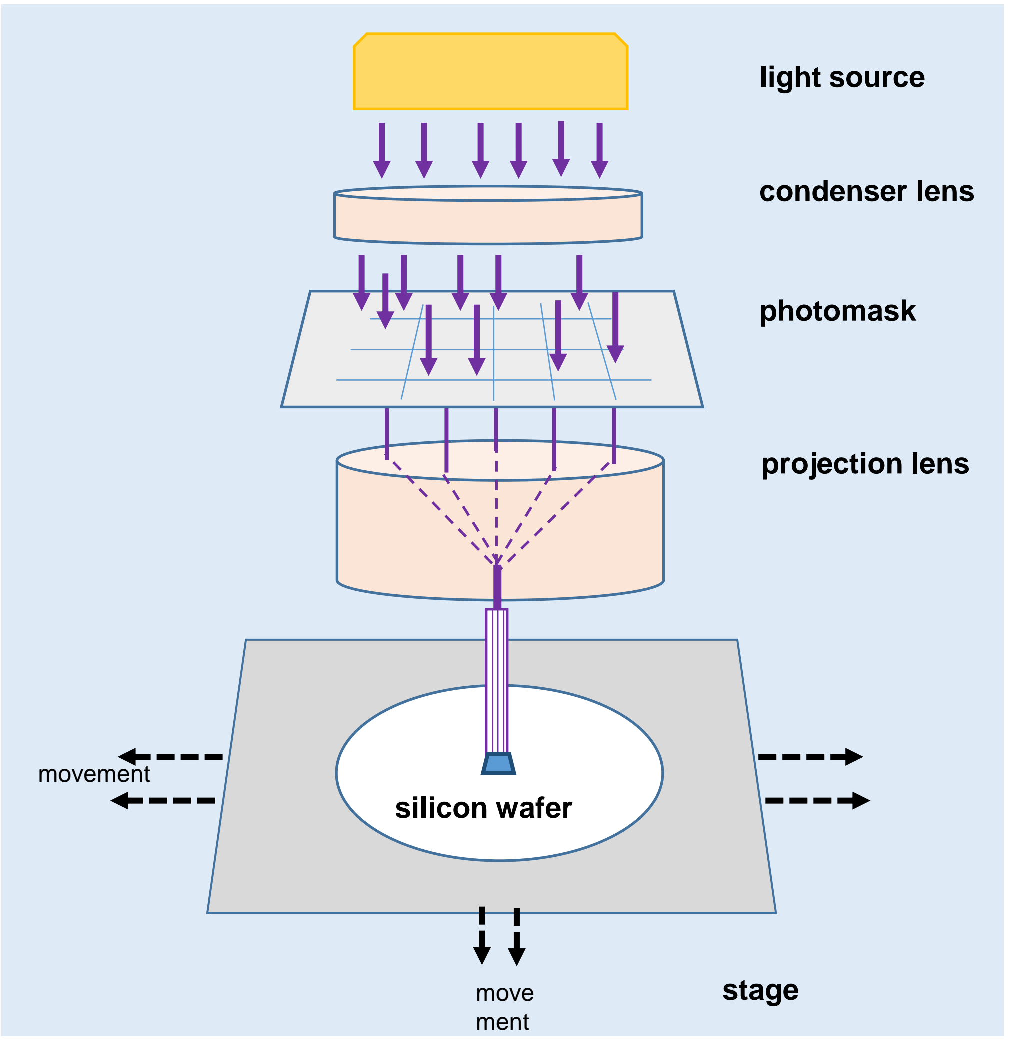
EUV light source for even shorter wavelength (13.5nm)

Realization of further miniaturization of semiconductors

Shorter wavelengths for semiconductor lithography equipment light sources

Shortening the wavelength of the light source for semiconductor lithography equipment

1970s-early 1980s	g-line	436nm
From mid-1980s	i-line	365nm
From Late 1990s	KrF	248nm
From 2000s	ArF	193nm
From 2019	EUV	13.5nm



The metal hard mask is a "PVD film for the insulator etching process."

Copyright© 2024, ULVAC, Inc. All rights reserved

MHM : PVD Film for Etching Process

ULVAC's TiN Metal Hard Mask Technology

Copyright© 2024, ULVAC, Inc. All rights reserved

Changing device structures Our new technology

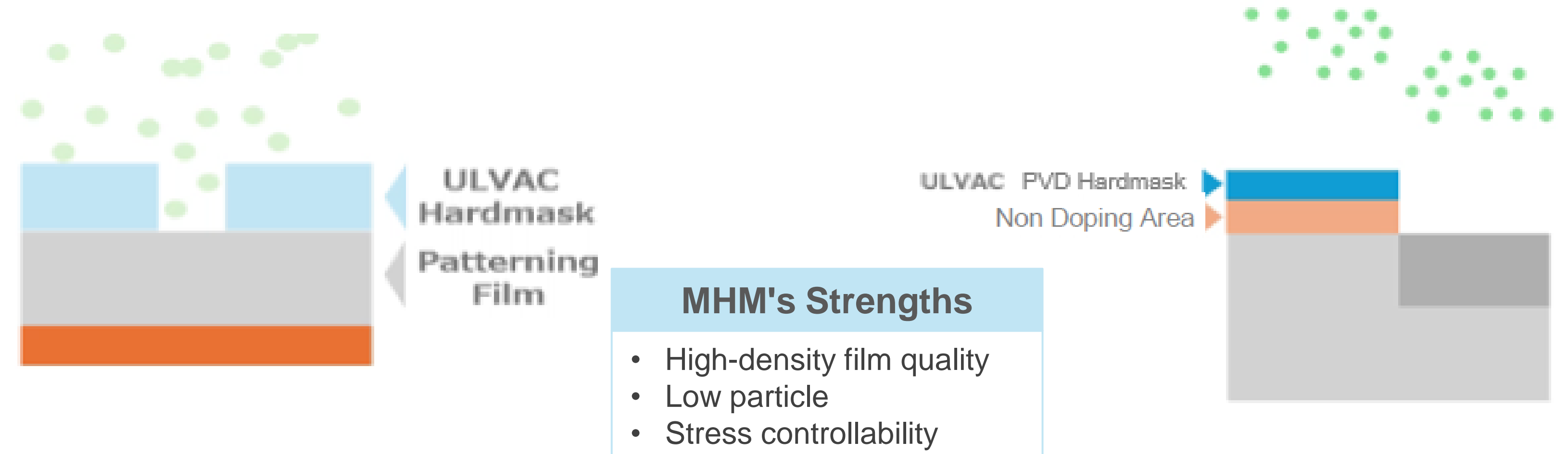
2018	2020	2022	2024 (Now)	2026	2028	2030	2032	2034	2036
7nm	5nm	3nm generation	2nm generation	A14	A10	A7	A5	A3	A2

Advanced devices start from Fin structure

Changes in Sheet Structure

Hardmask for Etching process

Adaptation of existing technology to backside wiring, New hardmask for diffusion process



MHM's Strengths

- High-density film quality
- Low particle
- Stress controllability

New Strengths of PVD

- Low temperature deposition
  No unnecessary diffusion
- No gas emissions
- Non-crystalline structure that does not lose its shape

Copyright© 2024, ULVAC, Inc. All rights reserved

PVD mask for diffusion process

Strengths of PVD in an increasingly complex complex process

1 Low temperature deposition	Reduction of heat load and diffusion
2 Crystallinity control	Control of film quality to suit the application
3 High-density, low-resistance film	High purity base film
4 Low impurity concentration	Reduction of pollution and degassing

Copyright© 2024, ULVAC, Inc. All rights reserved

PVD mask for diffusion process

Conventional Technology CVD Mask	Our PVD Masks
CVD Process	ULVAC Process(PVD)
CVD Hardmask	PVD Hardmask
Click Here!	Click Here!

Copyright© 2024, ULVAC, Inc. All rights reserved

Advantages of our PVD masks over conventional PECVD technology

The crystallization temperature of PVD masks is 600°C or higher. Mask performance can be maintained under thermal load conditions.

Intensity (a.u.)

111
220
311

800 °C
700 °C
650 °C
625 °C
600 °C
400 °C
As depo.

15
35
55
75

2θ (degree)

Maintains amorphous quality

Partially crystallized

As Depo.
10 1/nm

600°C
10 1/nm

>650°C
10 1/nm

Start of crystallization above 650°C

Broad, circular Electronics diffraction representing amorphous

PVD mask amorphous (hard to crystallize) Temperature resistance

(RTP X degree Ramp Up2min)

Copyright© 2024, ULVAC, Inc. All rights reserved

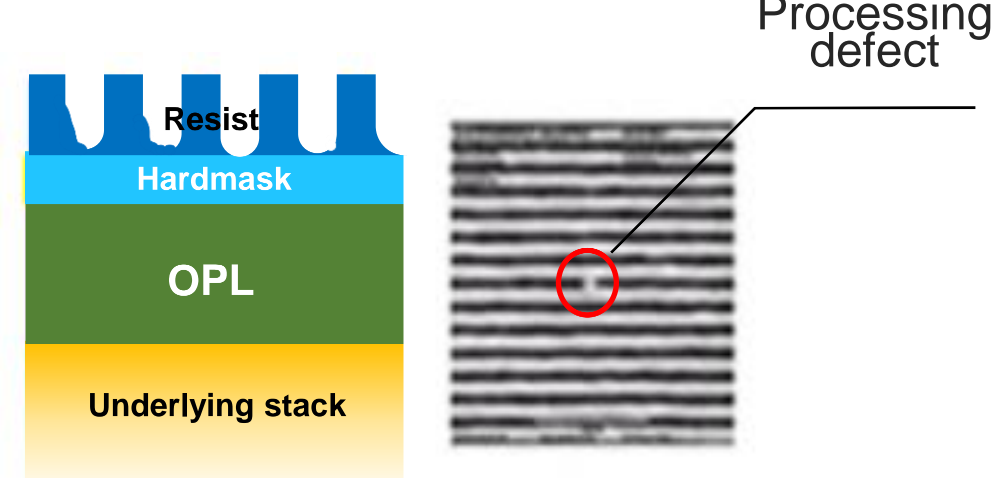
Problems with conventional technology CVD masks

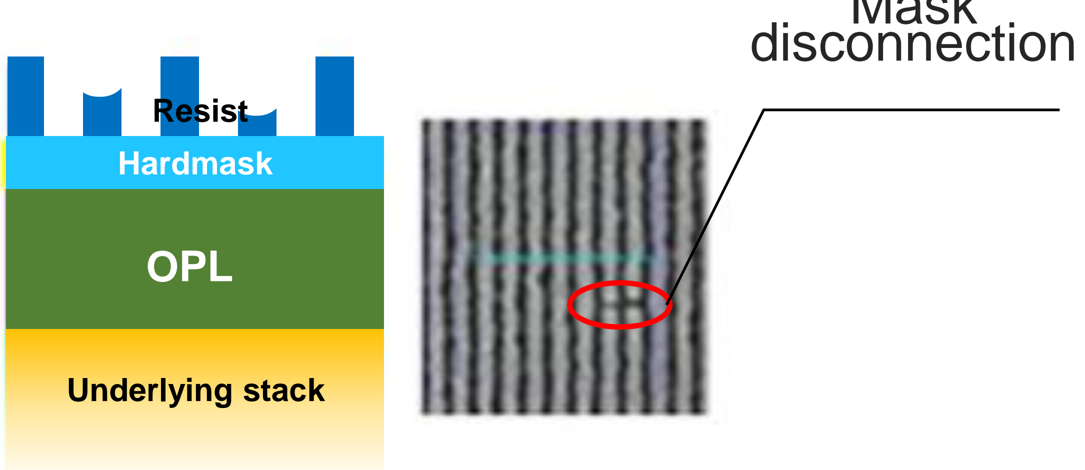
The problem with CVD masks is the adverse effects of released gases on photoresist.

Masks without gas emissions are needed for further miniaturization of sheet structure devices.

1) Due to emitted gas from CVD mask
Photoresist residue, processing defects

2) Due to emitted gas from CVD mask
Collapsed photoresist, processing failure





Source:.
De Silva et al.: Inorganic hardmask development for extreme ultraviolet patterning

Copyright© 2024, ULVAC, Inc. All rights reserved

Advantages of our PVD masks over conventional PECVD technology

- No emission of H_2 gas that adversely affects photo resist (same level as Bare Si substrates)
- Superior as Etching Mask

Gas emission characteristics in PVD mask As Depo (TDS Ramp rate 0.1°C/sec, max 600°C)

TDS Method Temperature rise conditions
Ramp rate =0.1°C/sec

Time (sec)	Temperature (°C) axis
0, 2,000, 4,000, 6,000, 8,000	0, 100, 200, 300, 400, 500, 600, 700

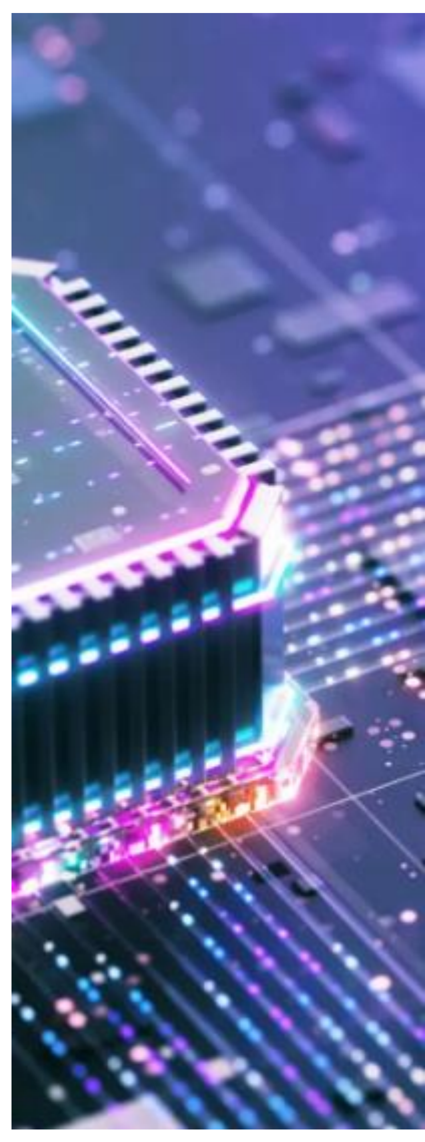
H2 gas emission m/z =2 intensity (a.u.)

1.0E-08, 1.0E-09, 1.0E-10, 1.0E-11

- PVD mask on Bare Si
- Bare Si

Temperature (°C): 0, 100, 200, 300, 400, 500, 600, 700

Copyright© 2024, ULVAC, Inc. All rights reserved



1. ULVAC PVD films and their strengths in a complex process
2. Our contribution in memory products for AI and adaptation of hardware
3. New Platform ENTRON-EXX

Copyright© 2024, ULVAC, Inc. All rights reserved

Semiconductor Business Progress in Memory Market

Order forecast

(Unit: $ billions)

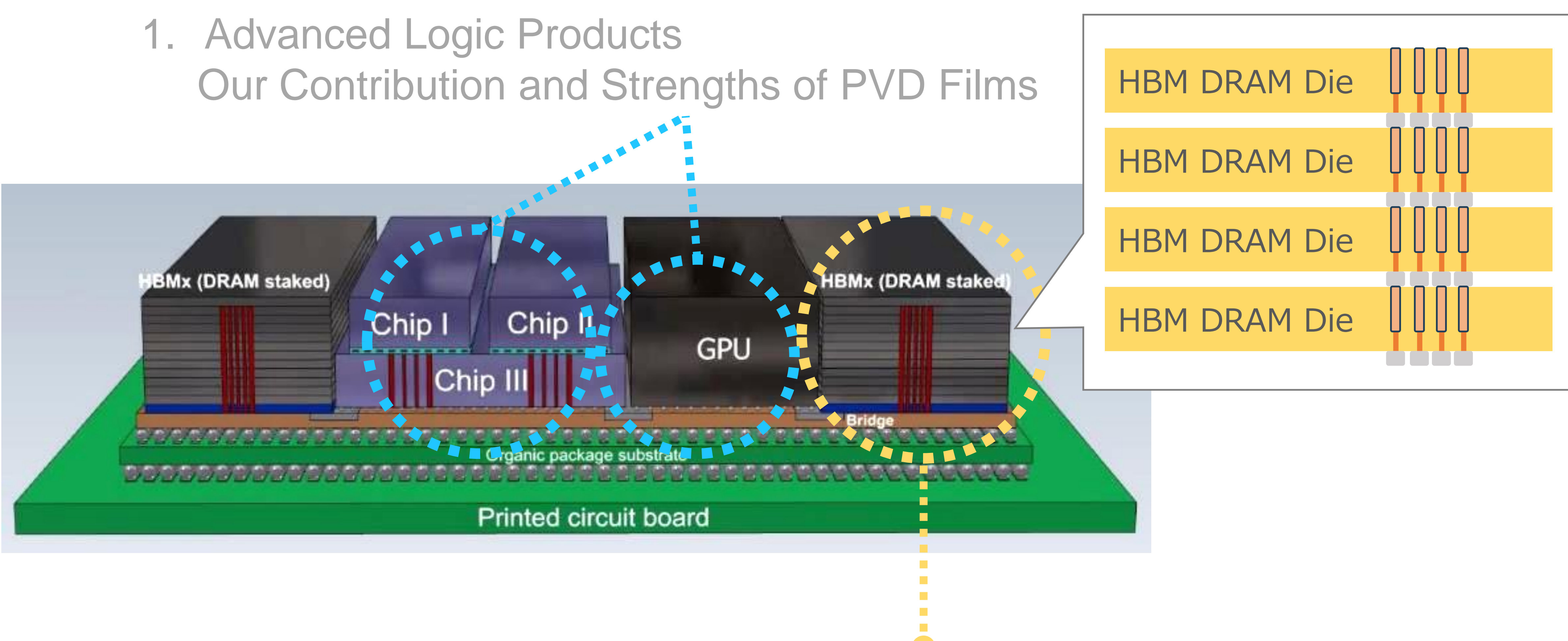
Contribution to BEOL's wiring process

Memory Progress
&
Further growth due to increase in number of customers and processes

Copyright© 2024, ULVAC, Inc. All rights reserved

Advanced AI Chipsets Required Semiconductor Products and Technologies

ULVAC



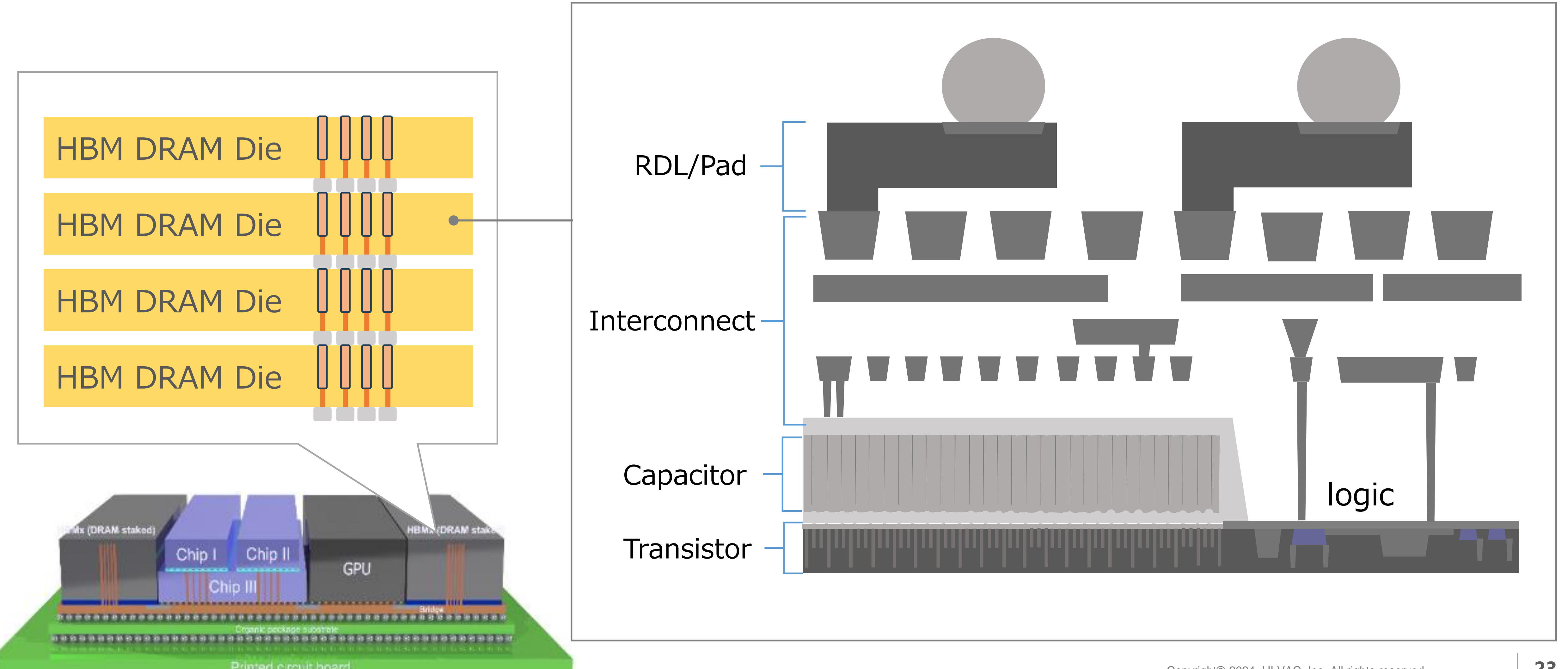
2. HBM (layered memory) for AI processors
Our Contributions and Strengths

Copyright© 2024, ULVAC, Inc. All rights reserved

Continuous process acquisition and development in Memory (DRAM)

ULVAC

In addition to HBM, process acquisition activities for conventional DRAM (DDR5) are in progress.
⇒Steady increase in number of processes



Copyright© 2024, ULVAC, Inc. All rights reserved

Adapted to Wafer Level Package from contribution in HBM (layered memory)

ULVAC

Response to thin wafer, warpage, and sagging in addition to process support
Planarization and temperature control technology utilized to back-end process and Wafer Level Package

Copyright© 2024, ULVAC, Inc. All rights reserved

1. ULVAC PVD films and their strengths in a complex process
2. Our contribution in memory products for AI and adaptation of hardware
3. New Platform ENTRON-EXX

Copyright© 2024, ULVAC, Inc. All rights reserved

Equipment name: ENTRON EXX

① Plug-In Platform connection simplification

② Software Extensibility

③ Designed with environmental impact in mind

Copyright© 2024, ULVAC, Inc. All rights reserved

① Plug-In Platform connection simplification

⇒Reduce relocation and remodeling turnaround time by **50%**

- ☐ Simplified chamber connections
- ☐ Simplified connection of essential facilities

Introduction of new equipment ENTRON-EXX

② Software Extensibility

Software to support operators

- Prevent human error (Parameter, Recipe)

AI

- Process parameter Optimization

Data

Analysis

Optimize

Playback Function

- Minimize Tool Down time

Data Visualization

- Tool Healthy monitoring

Copyright© 2024, ULVAC, Inc. All rights reserved

③ Sustainability

Designed with environmental impact in mind

- **20%** reduction in power consumption in standby mode
- **Up to 10%** reduction of installed floor space in clean rooms
- Regular maintenance consumables are fully compatible with conventional models
- Sputtering target recycling program under consideration

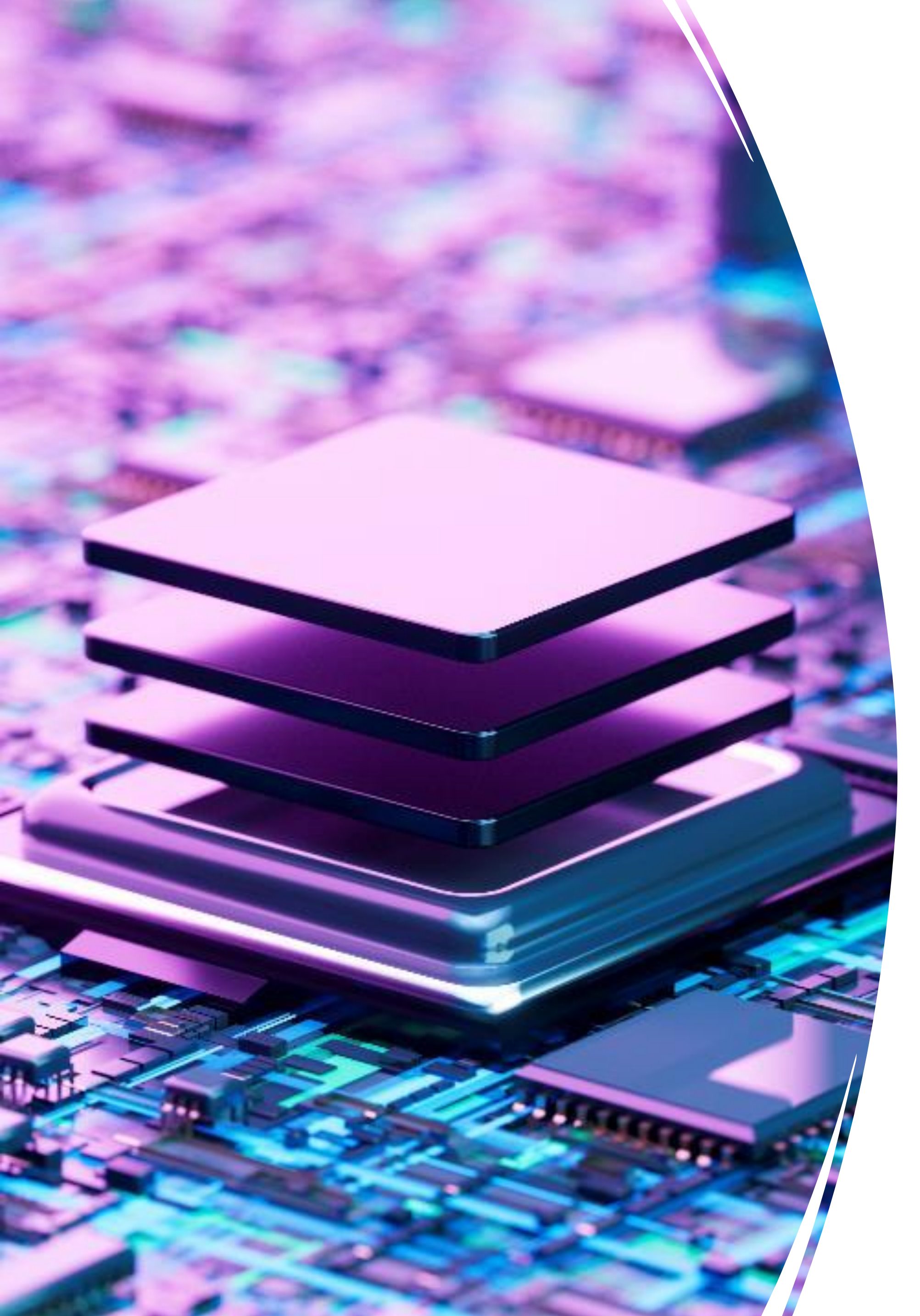
Copyright© 2024, ULVAC, Inc. All rights reserved

Technology Center

Technology Center PYEONGTAEK, Pyeongtaek, Korea

Opening Ceremony

Copyright© 2024, ULVAC, Inc. All rights reserved



State of Advanced Packaging and Our Approach

Executive Officer, General Manager of Advanced Electronics Equipment Division, Equipment Business HQ
Harunori Iwai

Business Planning Department, Advanced Electronics Equipment Division, Equipment Business HQ
Junya Kubo

1. About Advanced Packaging
2. Interposer and Descum processing
3. Panel Level Packaging and Our Surrounding Environment

Copyright© 2024, ULVAC, Inc. All rights reserved

Elements required for AI semiconductors

Semiconductor miniaturization

Adoption to HBM

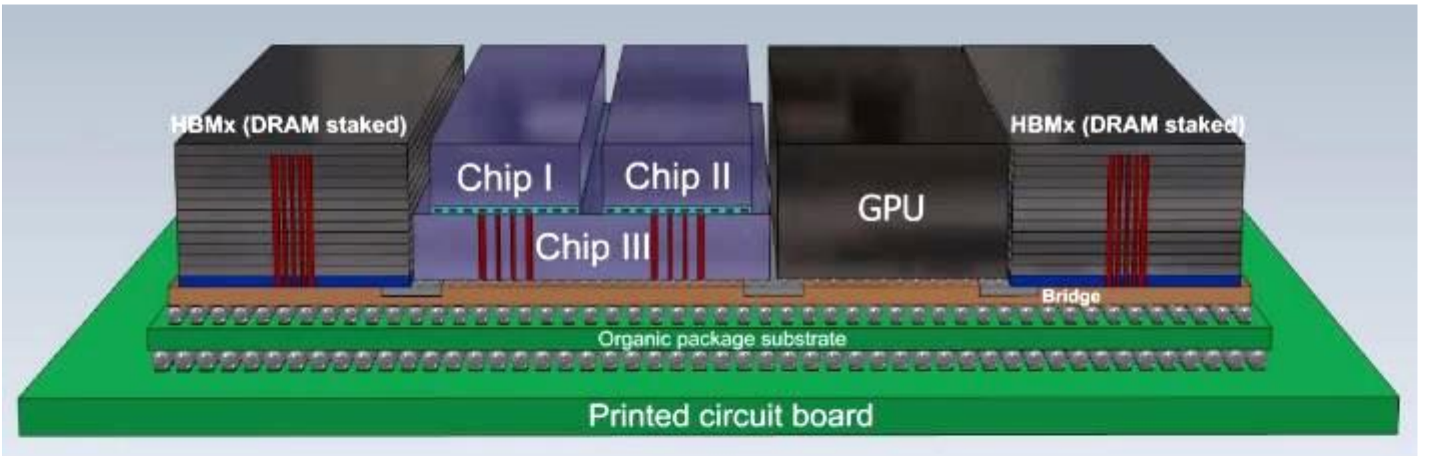
Application of new materials

Application of new structure

Copyright© 2024, ULVAC, Inc. All rights reserved

Role of Advanced Packaging and Evolution of Technology

Role of Packaging (fine, short, high-density connection of wiring)



Evolution of Packaging Technology

Existing Packaging

Advanced Packaging

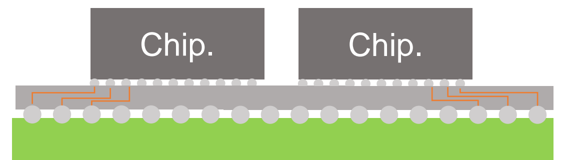
- ✓ Lay out individual chips

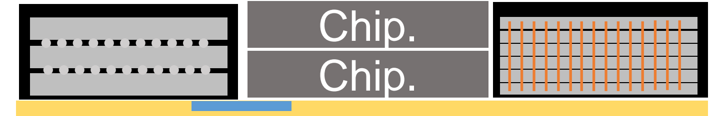
- ✓ Multiple chips side by side on the same substrate
  →Short and dense wiring

- ✓ Mounting Chips directly on the chip
  →More memory in multiple stages
- ✓ Use materials other than Si such as resin, glass, etc.

Chip.

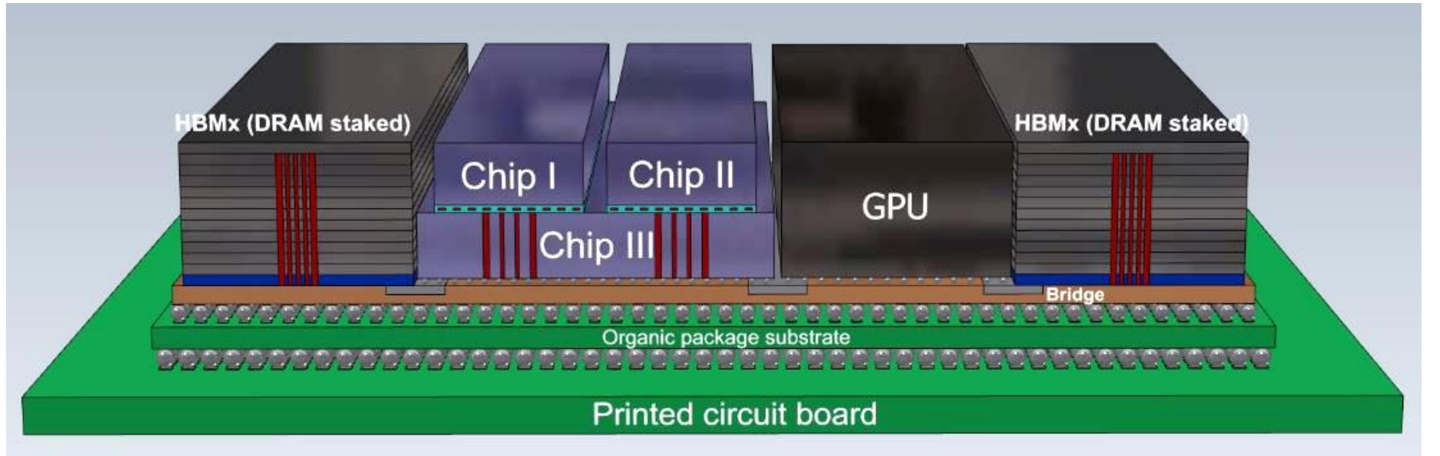
Chip.





Copyright© 2024, ULVAC, Inc. All rights reserved

Our technologies used in advanced semiconductor packaging



- Plasma Dicing
- TSV etching (through-silicon substrate processing)
- Etching for glass processing (optical waveguide formation)
- TGV Glass substrate hole etching
- Etching for microfine patterning

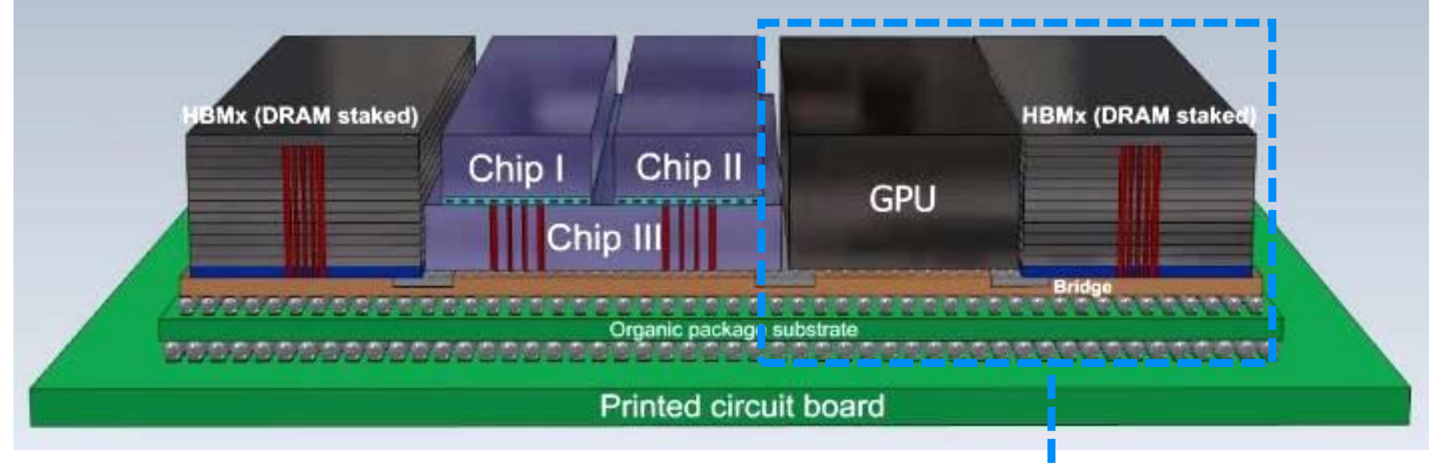
- Plasma surface activation (hybrid bonding)
- Electrode formation sputtering
- Seed sputtering for packaging substrates
- Desmear treatment for packaging substrates
- Descuming for interposer

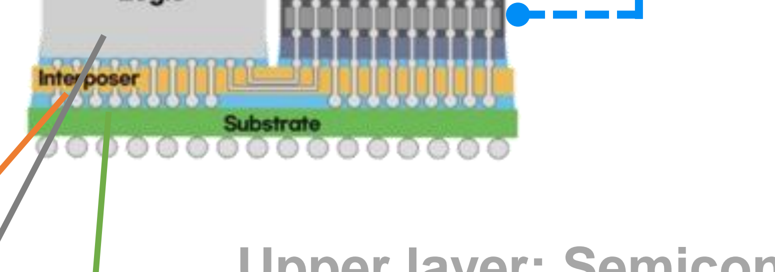
Copyright© 2024, ULVAC, Inc. All rights reserved

1. About Advanced Packaging
2. Interposer and Descum processing
3. Panel Level Packaging and Our Surrounding Environment

Copyright© 2024, ULVAC, Inc. All rights reserved

What is an interposer?





Interposer
HBM
Logic
HBM
HBM
HBM

Upper layer: Semiconductor chip

Middle layer: Interposer

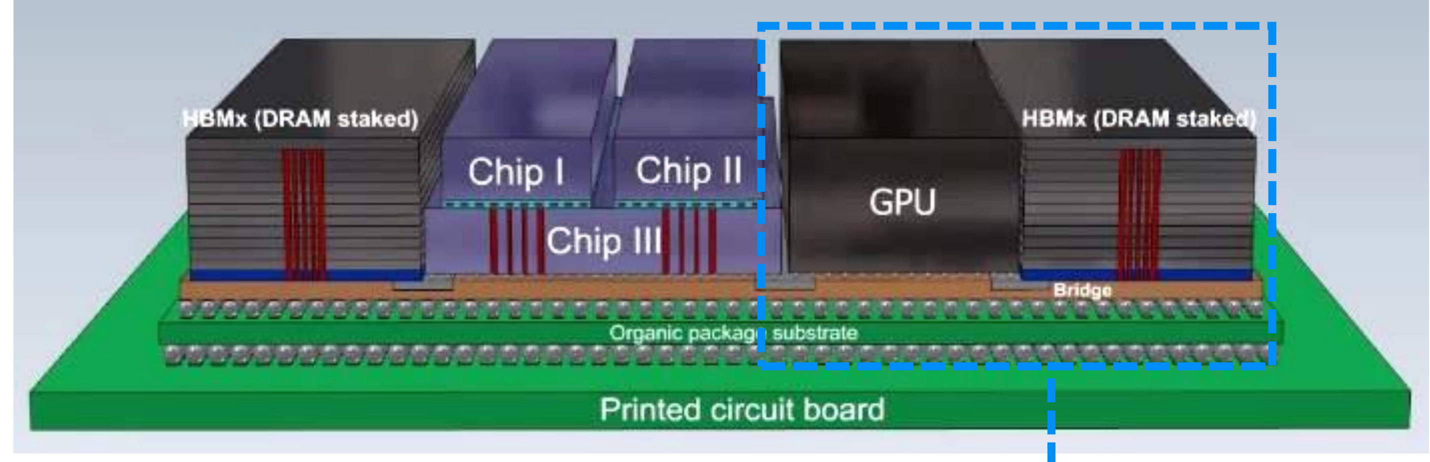
Lower layer: Packaging substrate

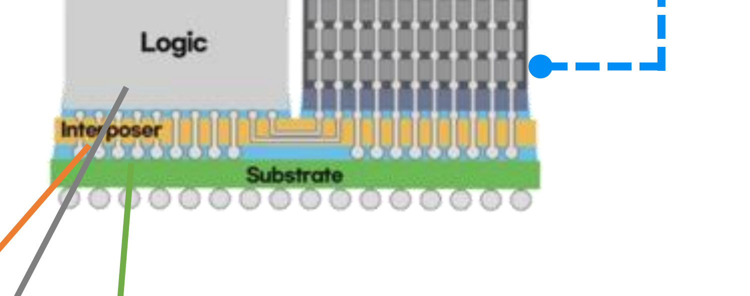
Interposer Functions

- Streamlining Connections
- Space Savings
- Signal quality improvement
- Improved thermal management

Copyright© 2024, ULVAC, Inc. All rights reserved

Interposer Technology Trends





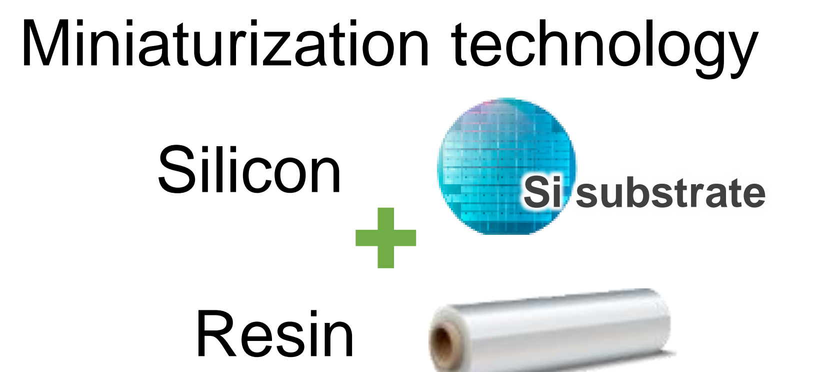
Interposer
HBM
Logic
HBM
HBM
HBM

Upper layer: Semiconductor chip

Middle layer: Interposer

Lower layer: Packaging substrate

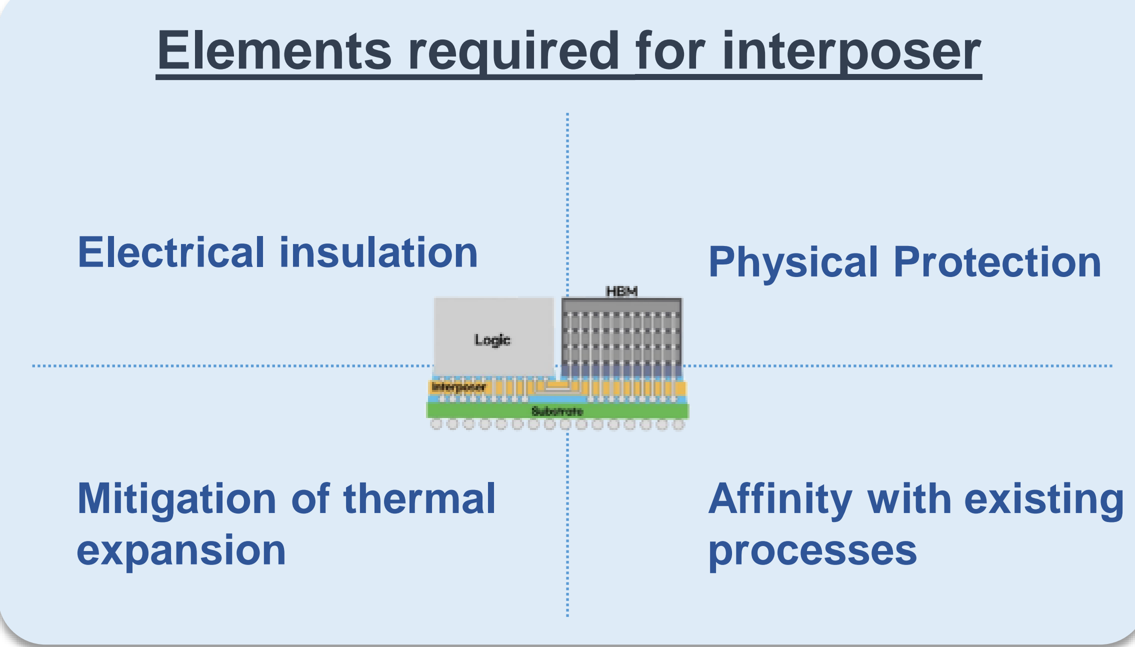
Interposer materials



Diverse Approaches
utilizing the characteristics of resin and silicon

Copyright© 2024, ULVAC, Inc. All rights reserved

Role of the interposer



Elements required for interposer

Electrical insulation

Physical Protection

Mitigation of thermal expansion

Affinity with existing processes

Unstable elements due to resin characteristics

Thermally unstable

Chemical instability

Variation of mechanical properties

Precision processing required

The material that fulfill these roles

Resin

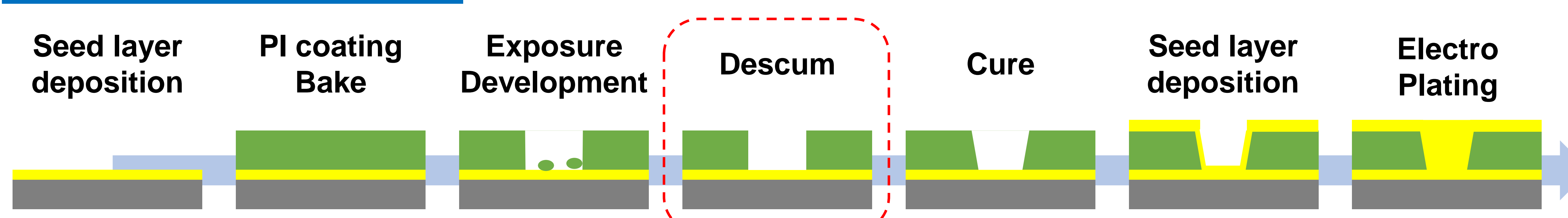
No damage to the resin allowed

Selection of optimum process equipment is essential

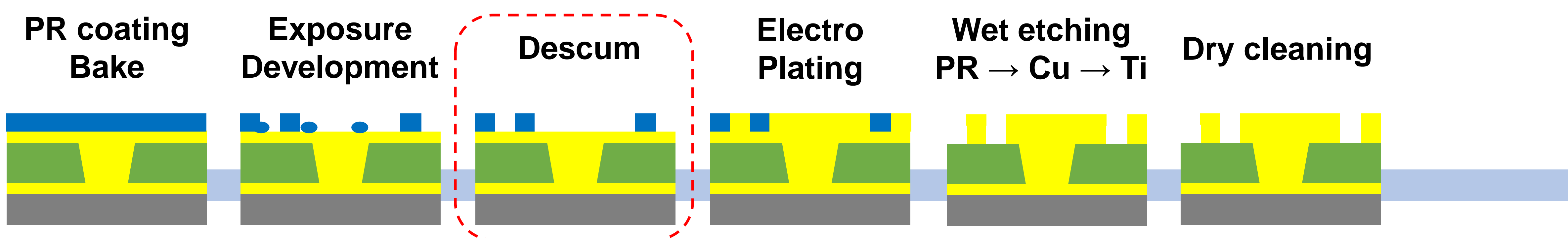
Copyright© 2024, ULVAC, Inc. All rights reserved

Main processes in which our equipment is used

Via Production Process



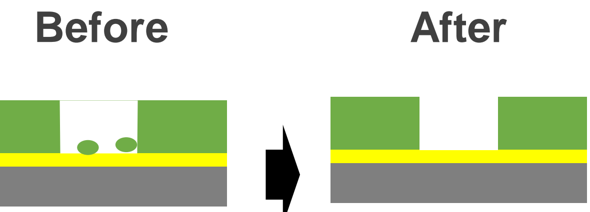
Wiring Fabrication Process



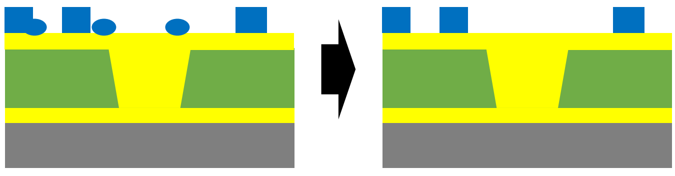
Copyright© 2024, ULVAC, Inc. All rights reserved

Example of implementation in our descuming equipment

Before After



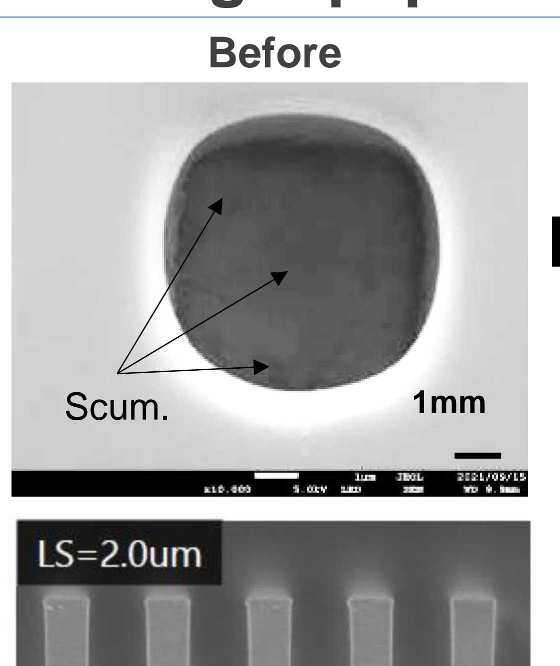
While retaining its shape
Remove residue

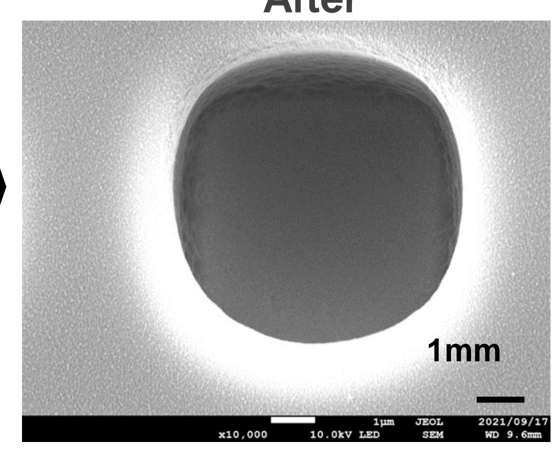


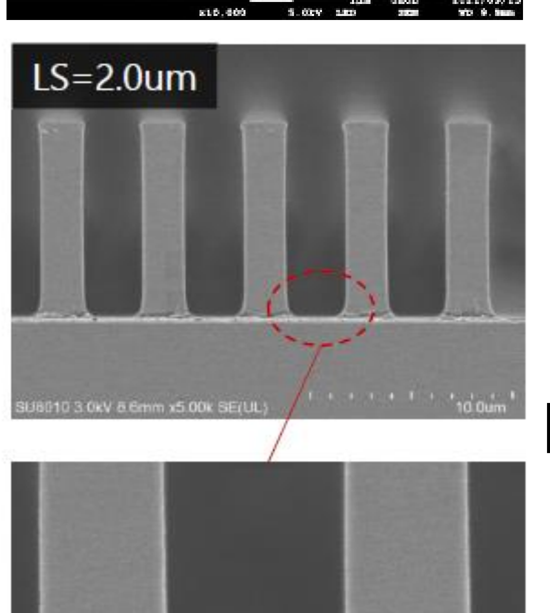
Gently remove only the inconvenient parts
Maintains resin properties

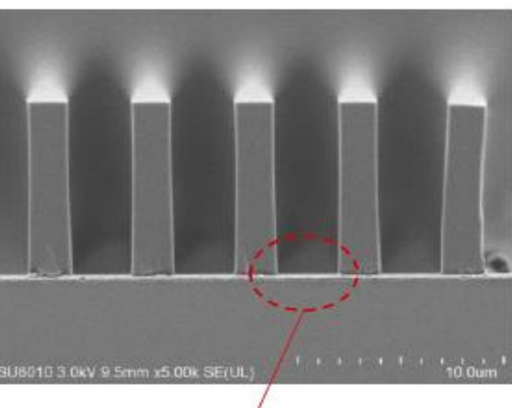
Plasma System
Model: NA

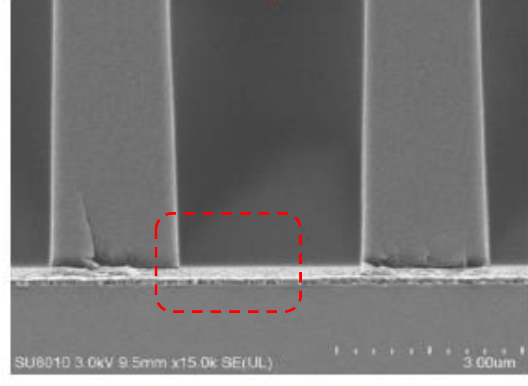
Before After









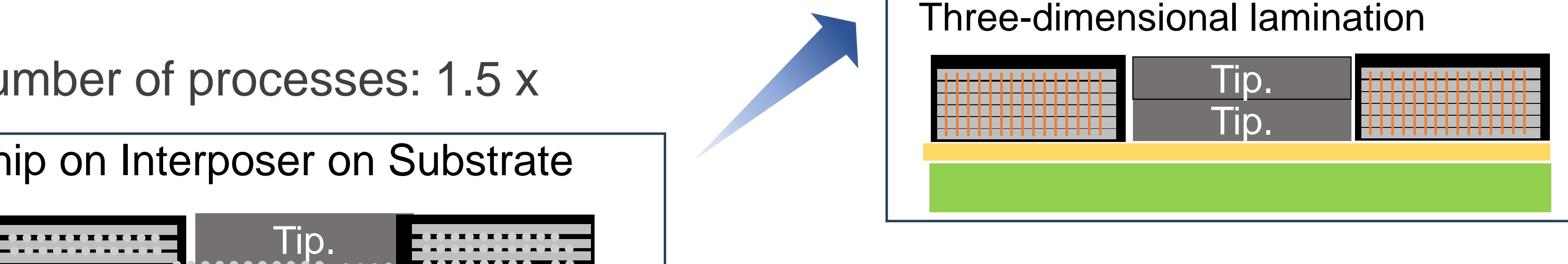


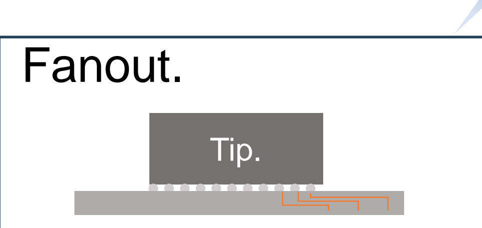
Number of Advanced Packaging Processes and Cumulative Shipments and Destinations

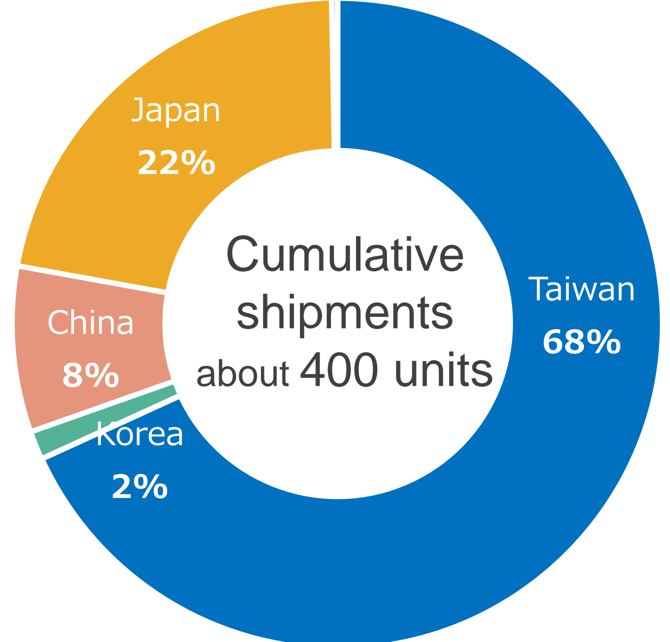
2015~ | 2023～ | 2026～

Number of processes 1.5 x+ α

Number of processes: 1.5 x





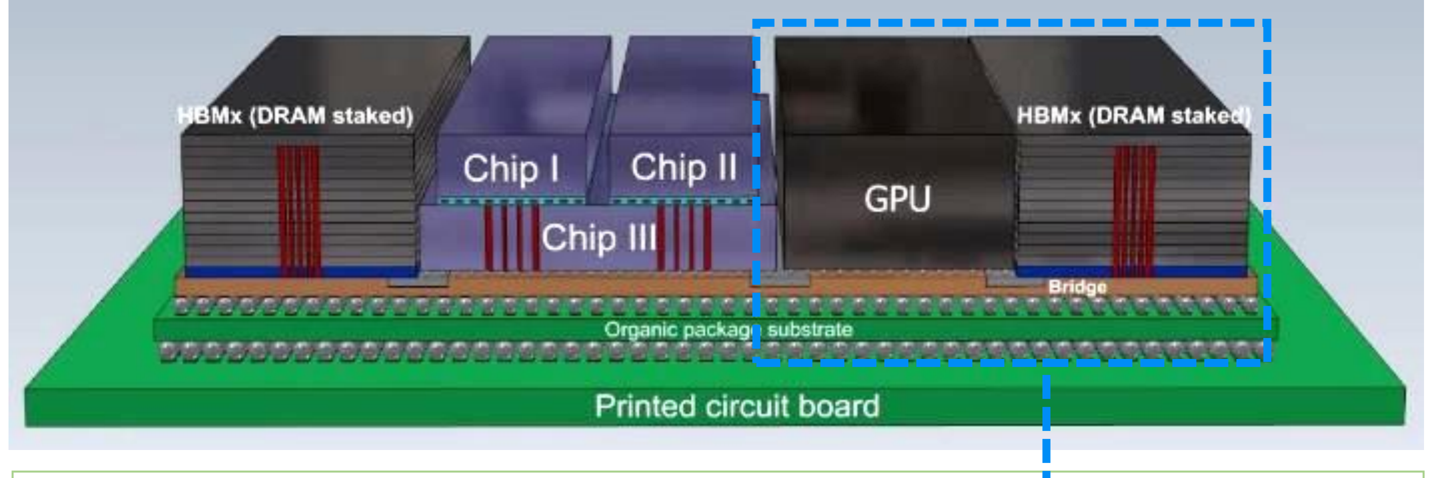


Copyright© 2024, ULVAC, Inc. All rights reserved

1. About Advanced Packaging
2. Interposer and Descum processing
3. Panel Level Packaging and Our Surrounding Environment

Copyright© 2024, ULVAC, Inc. All rights reserved

Technology Trends in Packaging Substrates



HBM

Logic

Interposer

Substrate

Interposer
HBM
Logic
HBM
HBM
HBM

Upper layer: Semiconductor chip

Middle layer: Interposer

<u>Lower layer: Packaging substrate</u>

Challenges in packaging substrates

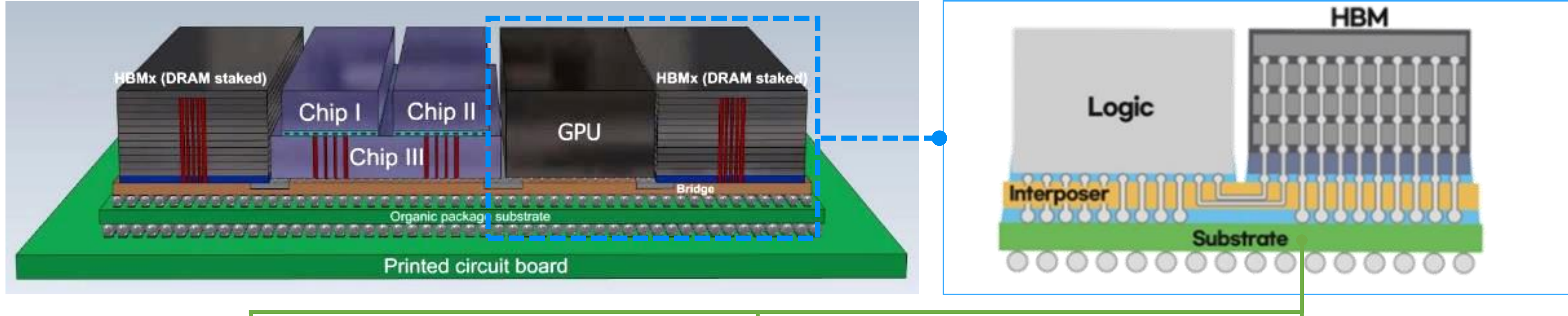
Resin

WET process ⇒ DRY process

Resin ➡ Glass

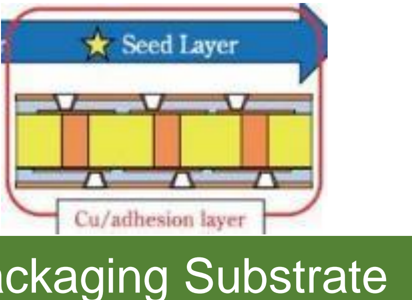
Copyright© 2024, ULVAC, Inc. All rights reserved

Contribution to PLP (Panel Level Packaging) process



■ Electrode formation for panel

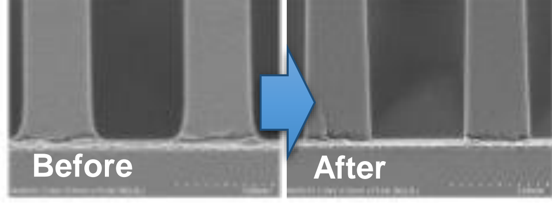
» Formation of metal thin film for electrode on large size substrate



Packaging Substrate

■ Descum

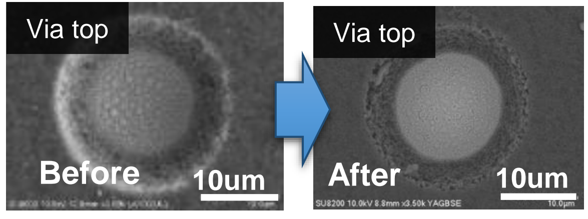
» Residue removal after litho of photosensitive materials



Large Interposer

■ Desmear

» Removal of residue after laser processing



Packaging Substrate

Copyright© 2024, ULVAC, Inc. All rights reserved

Panel Level Process History of Initiatives

	2011～	2018~	2024~.

Interposer

- Seed Sputter — R&D
- Descum — R&D

8sets

Packaging Substrate

- Seed Sputter — R&D
- Desmear — R&D

16sets

Plasma system for panels
NA-1500

Sputtering equipment for panels
SMV-500

Total
24sets

Copyright© 2024, ULVAC, Inc. All rights reserved

Tackling the PLP Challenge with the Collective Strength of the Group

ULVAC

Semiconductor

Proven in production

- 300φ Sputter
- Logic (Metal Hard mask)
- Cu RDL
- Low-Particle

Flat Panel Display

Proven Industry Leader

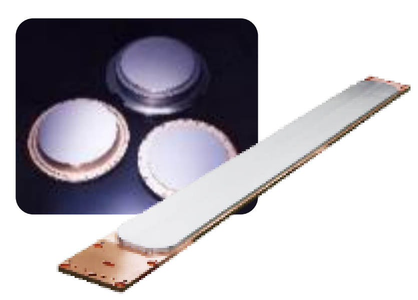
- Large Size Sub. (400mm~3000mm)
- Glass Transfer
- PI/Glass Carrier transfer

Adv. Electronics

flexibility of system concept

- Surface Modification
- Organic Sub.
- Curved Sub.
- Glass Transfer
- PI/Glass Carrier transfer

Material



Various Materials

- Pure Tungsten
- Cu Alloy, Cu, MoTi,,,,
- Oxide material
- Adhesion Metal

Panel Level Package

Copyright© 2024, ULVAC, Inc. All rights reserved

Packaging-related consortiums

Participation in US-JOINT, a consortium of 10 Japanese and U.S. companies in materials, equipment, etc., established in July 2024

tok

Copyright© 2024, ULVAC, Inc. All rights reserved

Expand growth of Semiconductor & Packaging business

Semiconductor & Packaging Long-Term Order Targets

Copyright© 2024, ULVAC, Inc. All rights reserved

ULVAC