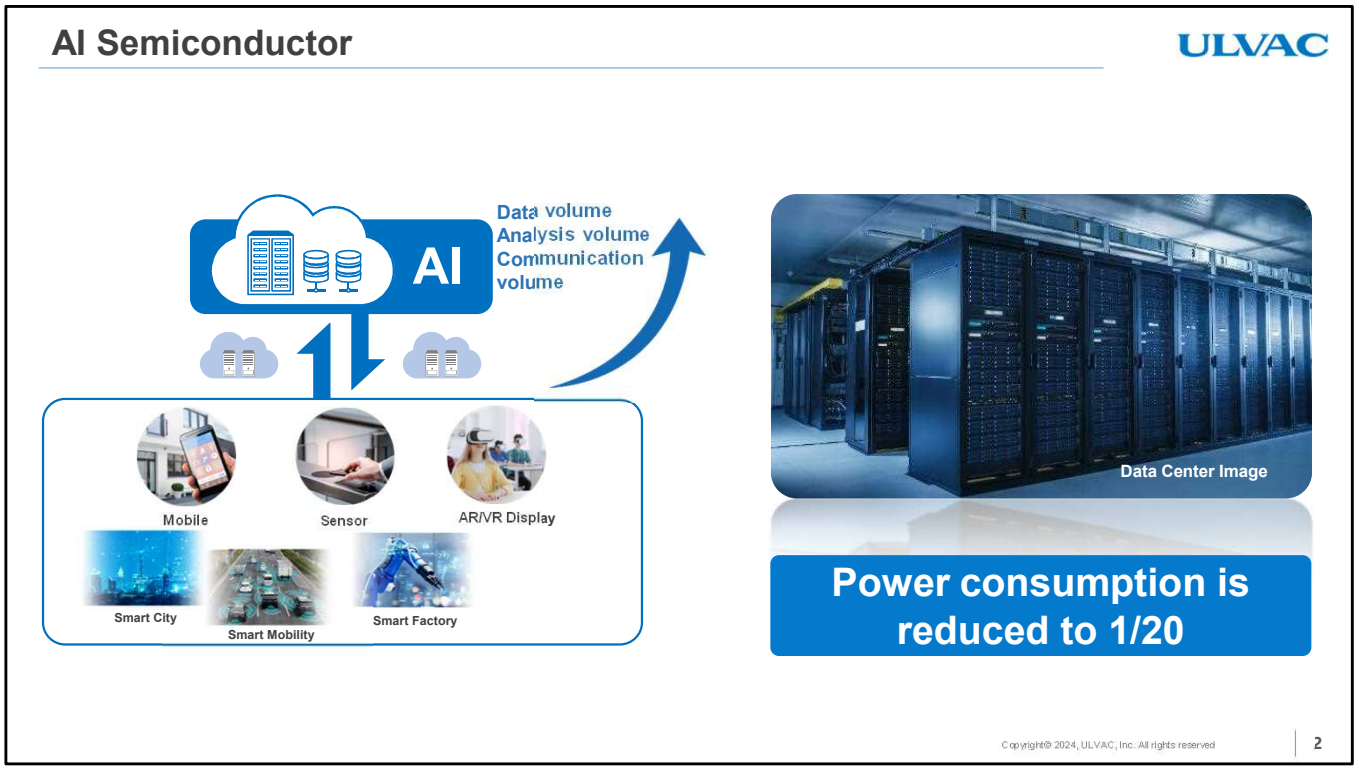
Hello, everyone. I am Harada from the IR Division of ULVAC. Thank you very much for attending our IR seminar today.

I will go straight to introducing today's agenda.

In this presentation, entitled “Expansion of Semiconductor Electronics Business Pioneered by Generative AI,” we will introduce technology trends in logic and memory and our approach, as well as the current status of advanced packaging and our approach.



Before I get into the main topic, I would like to briefly discuss the background that led us to this theme.

AI semiconductors are expected to be used not only in servers but also in edge AI terminals to solve traditional problems and support various industries by quickly processing large amounts of information.

For example, image recognition cameras, medical diagnostic technology, and automated driving require the use of large amounts of information and instantaneous decision making. With the proliferation of IoT, the volume of data is increasing and real-time processing is required. AI technology will support these requirements, and computer chips for AI in particular will be extremely important.

AI semiconductors are components specifically designed for computers to think. By using these semiconductors, computers are better at processing more information at once and more quickly than ordinary components. AI semiconductors are smaller, faster, and operate with less power than conventional semiconductors combined. For example, it is said that AI data centers can reduce power consumption to 1/20 by using the latest semiconductors, and technology is evolving daily.

Miniaturization of semiconductors improves chip performance, and further advances in the substrates that the semiconductors are mounted on enable the AI semiconductors to maximize their performance.

What are AI Semiconductors?

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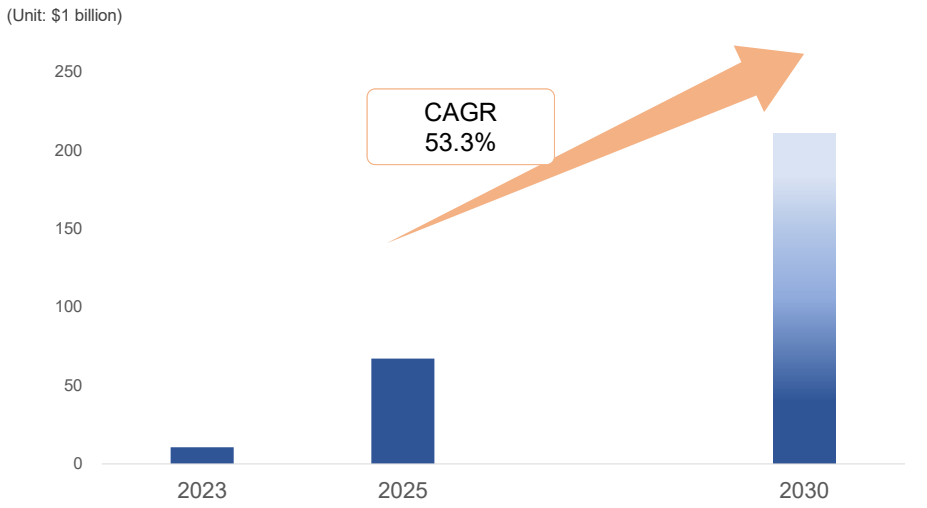
Generated AI Market Demand Forecast (Global)



Source: Japan Electronics and Information Technology Industries Association

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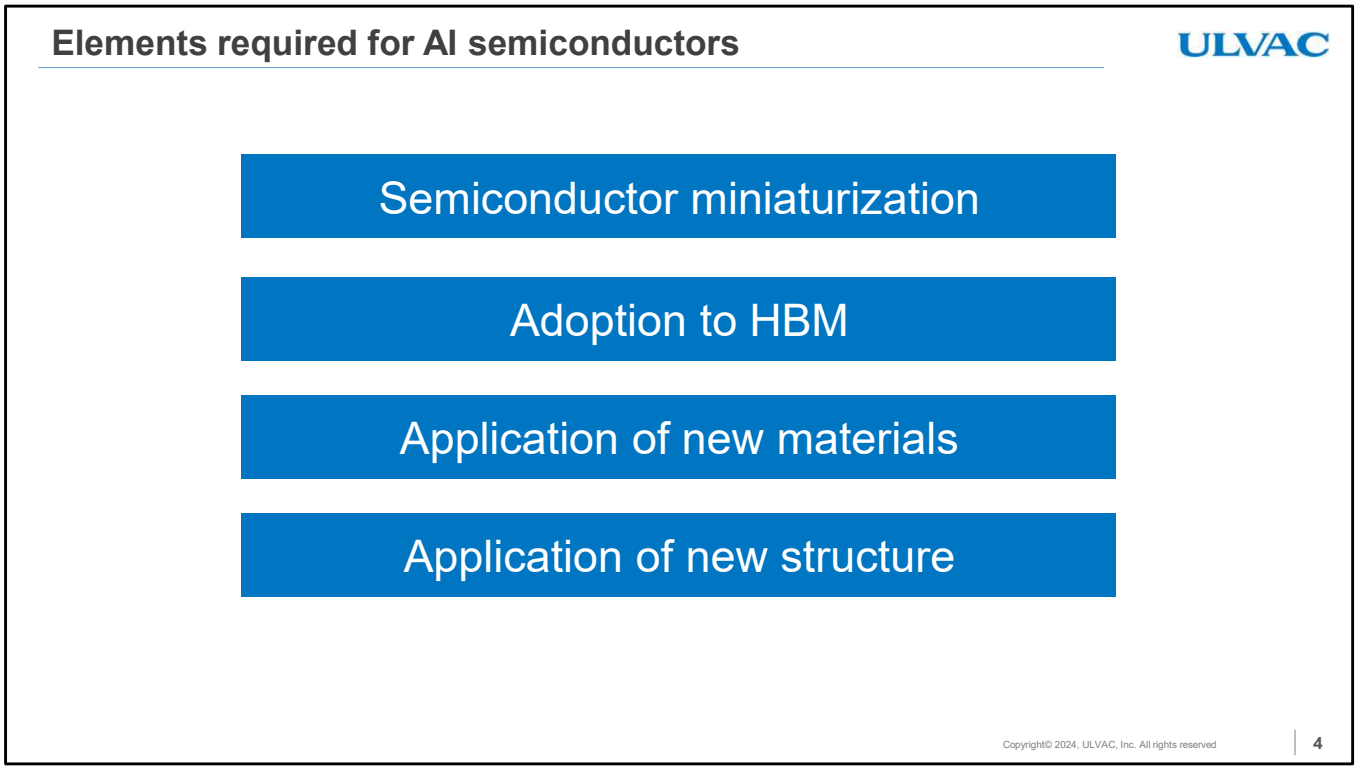
As cloud computing becomes more prevalent, AI-based services are increasing.

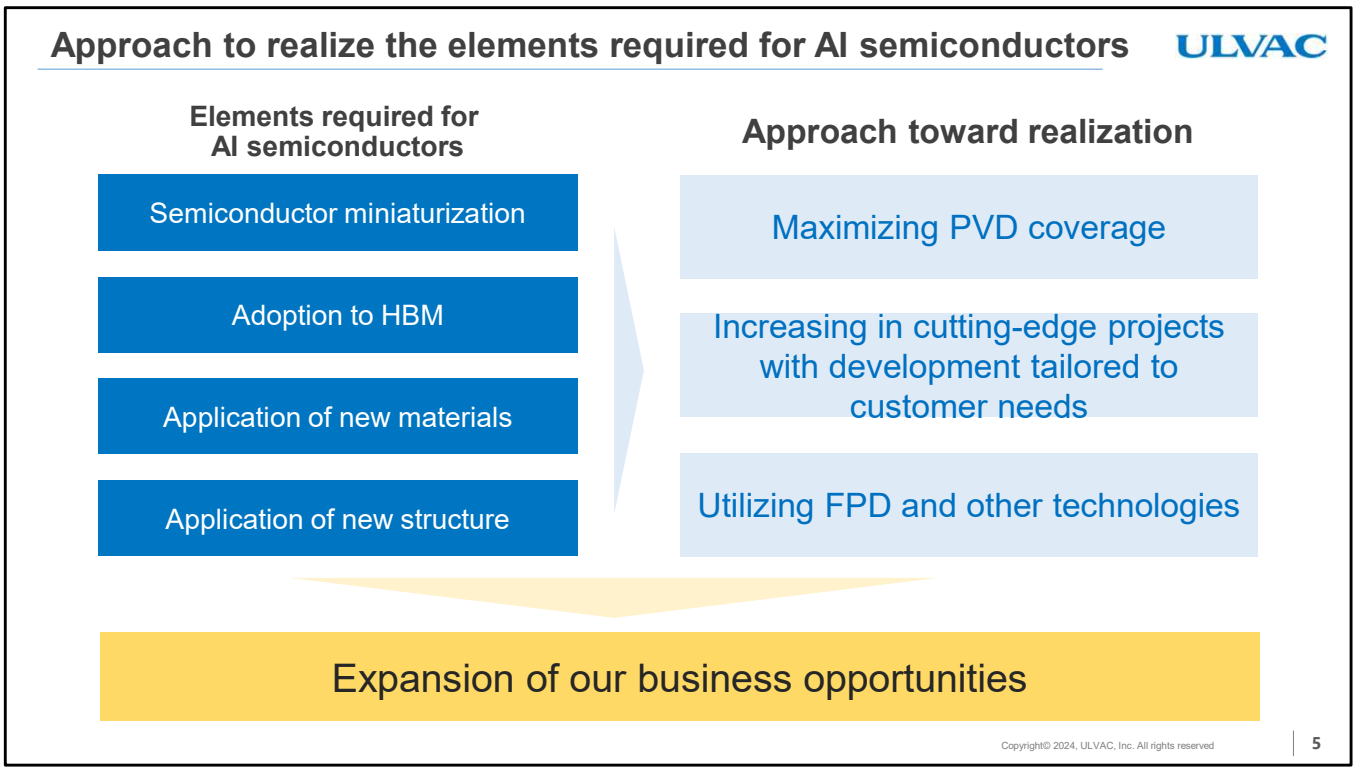
By around 2030, the generative AI market is projected to grow about 20 times bigger than in 2023, at an average annual growth rate of more than 50%. AI semiconductors are designed to operate efficiently for specific tasks, and their specialized nature has broadened their applications. Each manufacturer is developing its own semiconductors, and the market as a whole is expected to continue to grow as the range of applications expands.

Furthermore, advances in AI technology are expected to be used in new industrial fields and applications, a factor driving further market expansion.



Many different AI semiconductor chips specifically for a wide variety of applications have been developed. These chips address various challenges to achieve high speed, low power consumption, high efficiency, and reliability.

Factors required for AI semiconductors include miniaturization of chips, support for HBM to increase data transfer speeds, and application of new materials and structures.



We are taking various approaches to realize the elements required for AI semiconductors.

Specifically, we have developed a wide range of businesses with diverse technologies such as vapor deposition, CVD, and etching. At the same time, we are expanding the scope of application to new processes by taking advantage of the features of PVD technology, which is one of our strengths.

Furthermore, the number of cutting-edge projects is increasing as we develop close to our customers' needs. In addition, new business opportunities are expected to expand by leveraging FPD technology, a traditional strength of the Company.

As the generative AI market expands, demand for AI semiconductors is expected to increase, and the overall semiconductor market TAM is also expected to grow. Under these circumstances, we are implementing initiatives to embody the elements required for AI semiconductors and are also aiming to expand our market share.

Expand growth of Semiconductor & Packaging business

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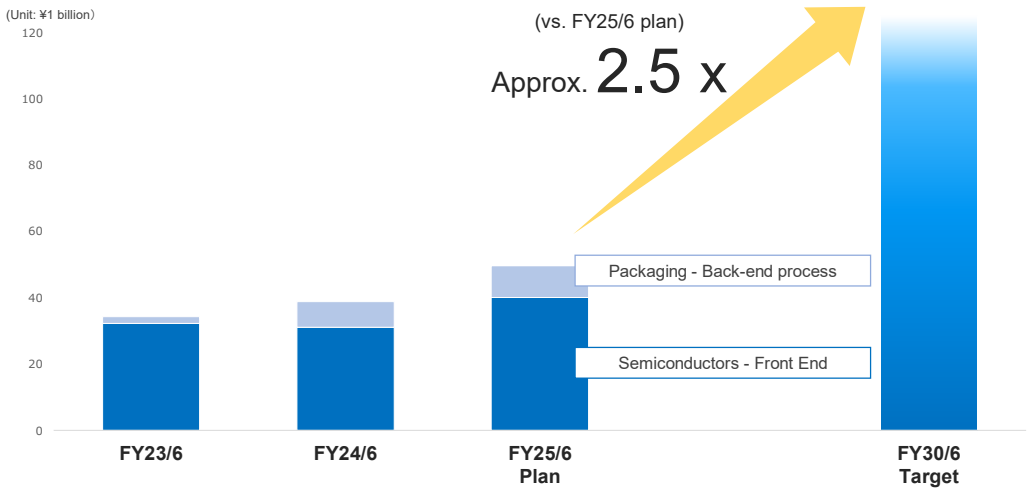
Semiconductor & Packaging Long-Term Order Targets



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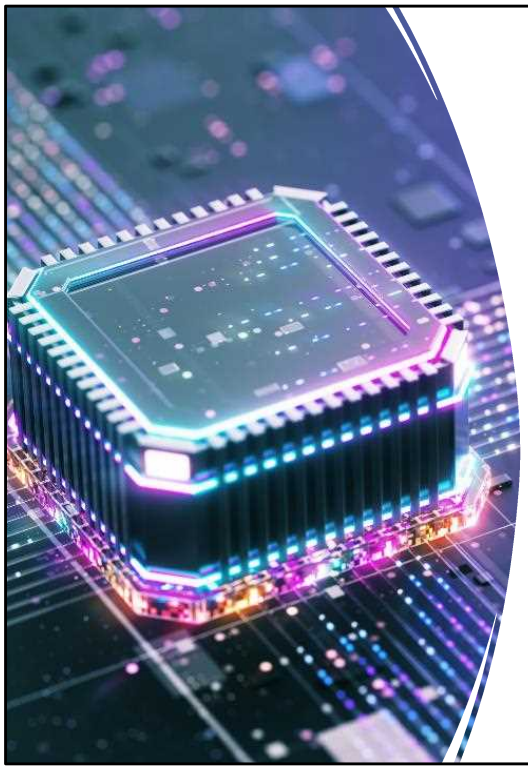
By aggressively pursuing these initiatives, we aim to expand the scale of orders in the semiconductor and packaging business to 2.5 times the current level, which exceeds the projected growth rate of the semiconductor market, by around 2030, or five years from now. We will also seek to improve our overall profitability by expanding our highly profitable semiconductor electronics business.

From hereon, we would like to introduce our efforts in the semiconductor electronics business to achieve growth and expansion. First, Mr. Iwasawa, Executive Officer Responsible for Semiconductor Marketing, will give an overview of the technology trends in logic memory and our efforts in this area.

Now, Mr. Iwasawa, please go ahead.



Logic and Memory Technology Trends and Our Approach

Executive Officer, Semiconductor Marketing
Hiroaki Iwasawa

I am Iwasawa of the Semiconductor Division.Now let me explain.

Elements required for AI semiconductors

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- Semiconductor miniaturization
- Adoption to HBM
- Application of new materials
- Application of new structure

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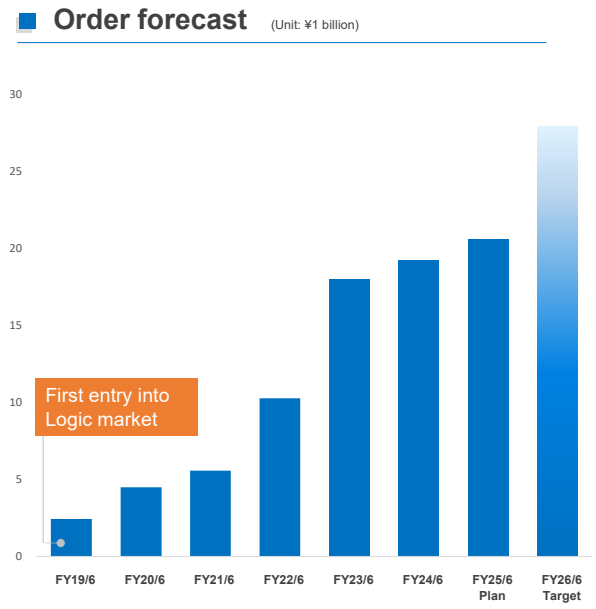
As mentioned previously, our company has contributed to the advancement of chip miniaturization, new materials and structures, which are the elements required for AI semiconductors. We believe we can continue to contribute to various processes. We have also entered into processes related to HBM and will continue to expand our processes..

Semiconductor Business Progress in Logic Market

ULVAC



Successful entry into the Logic market

- ✓ Expanding the number of customers
- ✓ From advanced EUV process to legacy product DUV process
- ✓ Expanding the adaptation of using a metal layer

Further growth due to increase in number of customers and processes

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Six years ago, we entered into the logic market with the adoption of metal hard masks in advanced logic.

Activities to widen market share to date have been focused on expanding equipment and processes adopted by leading-edge customers to other customers and other products. Equipment and processes that have proven their superiority in EUV lithography should also demonstrate their superiority in DUV lithography. The adoption of this equipment should be expanded in line with changes in device structure. Specifically, we have focused our support on increasing the number of processes that employ TiN, a metallic material, as an electrode material.

1. ULVAC PVD films and their strengths in a complex process
2. Our contribution in memory products for AI and adaptation of hardware
3. New Platform ENTRON-EXX

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From here, I would like to explain how our technology is being used in AI chipsets, which are nowadays the mainstay of development and mass production investments.

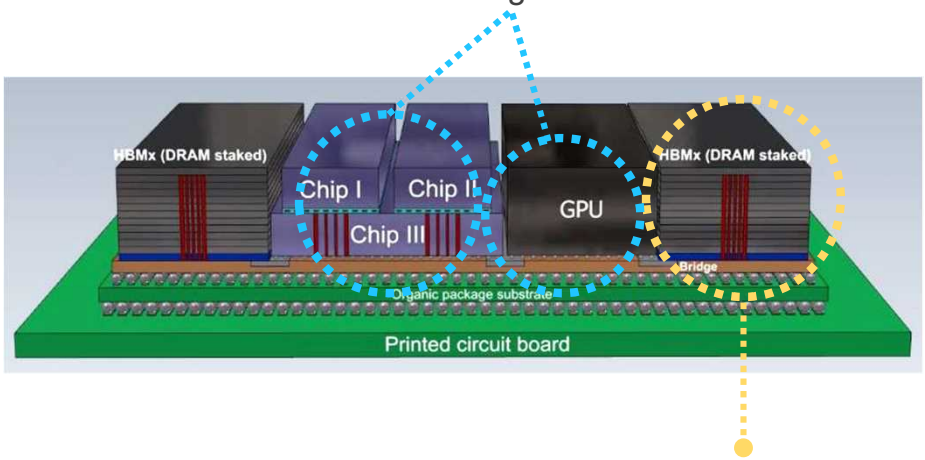
How are our PVD films being newly used in increasingly complex logic chip processes? We will explain what advantages we have over conventional processes and technologies.

Next, we will explain our contributions to memory products for AI chips and the details of improvements in equipment and hardware technology to be applied to memory for AI chips.

Next, we will introduce in turn our new equipment product, ENTRON-EXX, which we reported publicly last week. This ENTRON-EXX is a new platform that can install processes including the one we will introduce today with all-new hardware and software.

Advanced AI Chipsets:Semiconductor Products and Technologies Required ULVAC

1. Advanced Logic Products
   Our Contribution and Strengths of PVD Films



2. HBM (layered memory) for AI processors
   Our Contributions and Strengths

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This diagram schematically illustrates the structure of an AI chipset.
The main components in the front-end process are products of advanced logic represented by CPUs and GPUs, and the layered memory, or HBM. We will explain our contribution in the development and mass production of each of these products.

Contribution in Advanced Logic: EUV Adaptation Opportunities in Logic Market

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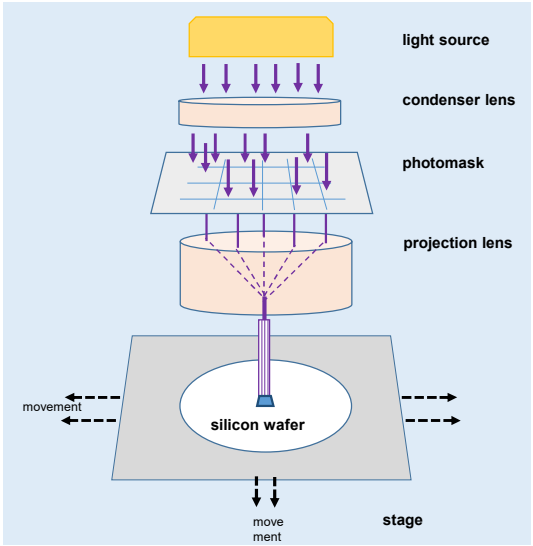
EUV light source for even shorter wavelength (13.5nm)

Realization of further miniaturization of semiconductors

Shorter wavelengths for semiconductor lithography equipment light sources

Shortening the wavelength of the light source for semiconductor lithography equipment

1970s-early 1980s	g-line	436nm
From mid-1980s	i-line	365nm
From Late 1990s	KrF	248nm
From 2000s	ArF	193nm
From 2019	EUV	13.5nm



The metal hard mask is a "PVD film for the insulator etching process."

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Once again, we have entered the logic market with TiN metal hard masks. Until now, the sputtering process has played a major role in the BEOL wiring process, directly depositing the wiring materials themselves, such as aluminum and copper. What I am talking about now is not the photomask of the lithography equipment, which is from the top in the figure on the right, but the metal hard mask, which is the equipment that deposits the mask on the silicon wafer.

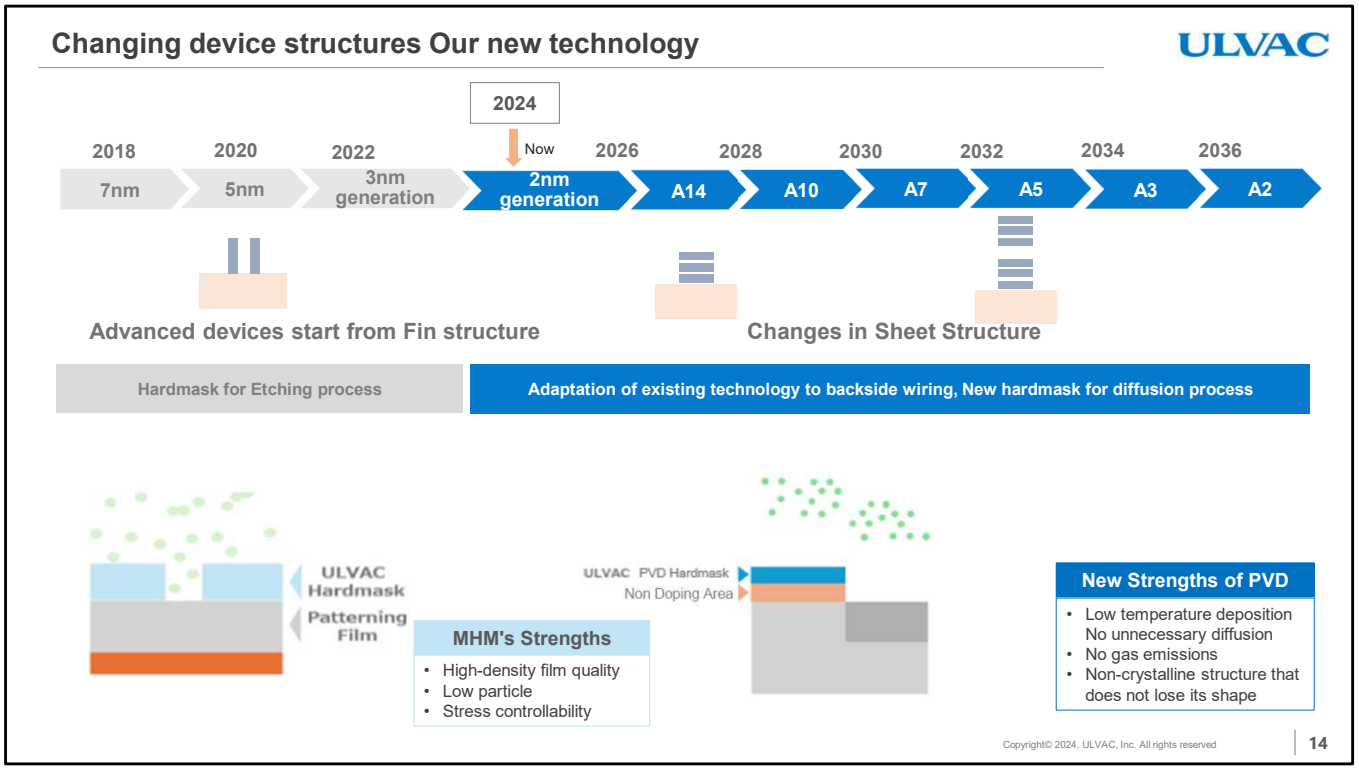
The TiN metal hard mask was an important step in expanding the possibilities of PVD technology beyond the role of conventional PVD equipment. TiN metal hard mask is a PVD film process optimized for the next process, etching, by taking advantage of the properties of high-density PVD films, adjustable initial stress, and low particle counts. Metal hard mask means a mask layer deposited by PVD for the next process, etching.

What you see here is a cross-sectional view of multilayer metal wiring. In this schematic diagram, the insulating film layer, which does not conduct electricity, is shown in white, and the copper wiring, which does conduct electricity, is shown in orange. How accurately and distortion-free the white insulating film layer can be processed is critical to the reliability of the wiring.

Our metal hard mask layer in red is deposited on top of the white insulating film that we want to etch precisely. Along with the resist of the light blue EUV lithography, our metal hard mask layer remains distortion-free and smooth even after being processed.

The etching process of the white insulating layer begins. Along with our metal hard mask in red, the white insulating layer was precisely processed. This is an example of how the hardness, smoothness, and lack of distortion of the PVD metal hard mask is transferred to the etching of the insulator layer in the next process.

In order for us to further expand our market share as a PVD vendor, we need to support our customers by understanding what characteristics are required of PVD films for the next process in a complex compound process.



In recent years, the structure of logic devices has reached a tipping point. The change from a Fin structure to a sheet structure has created new opportunities for equipment manufacturers, who have begun to develop their mass production. We have expanded our market share so far by having the metal hard mask process equipment used in Fin structures adopted for other applications with TiN as the metal material, and by applying it to backside wiring.

However, in order for us to further expand our market share, we need to move into new applications and new processes with new device structures. Therefore, today we would like to present our entry opportunity in a different process in the new device structure.

We have been given the opportunity to apply the low-particle, stable hardware that we have proven with TiN metal hard masks to other materials and other processes. Today, competition among PVD systems is still important, of course, but it is also important to take away processes from other processes, such as CVD processes, with PVD processes.

With PVD films for CVD, PVD films for ALT, PVD films optimized for CMP, PVD films optimized for lithography and various activities, we are aiming to triple the number of processes employed in logic.

PVD mask for diffusion process

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Strengths of PVD in an increasingly complex complex process

1 Low temperature deposition	Reduction of heat load and diffusion
2 Crystallinity control	Control of film quality to suit the application
3 High-density, low-resistance film	High purity base film
4 Low impurity concentration	Reduction of pollution and degassing

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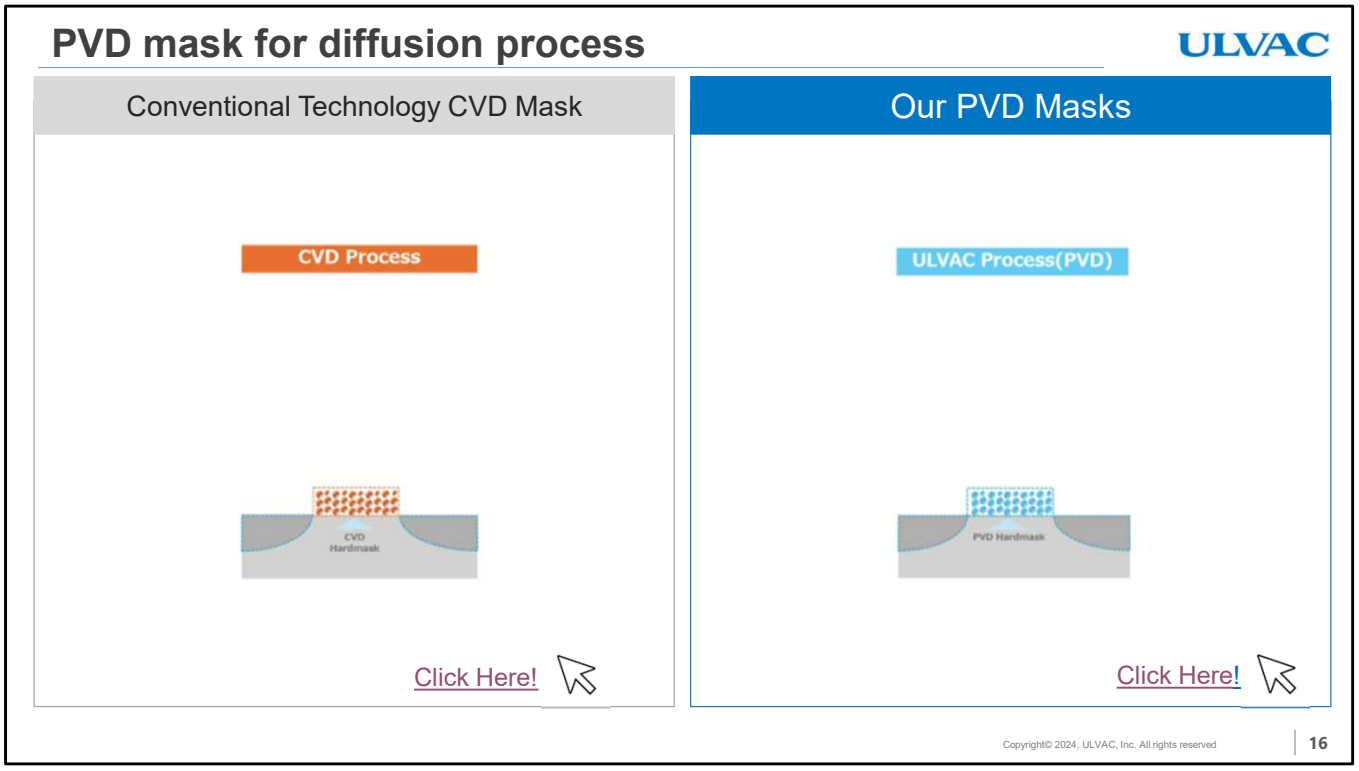
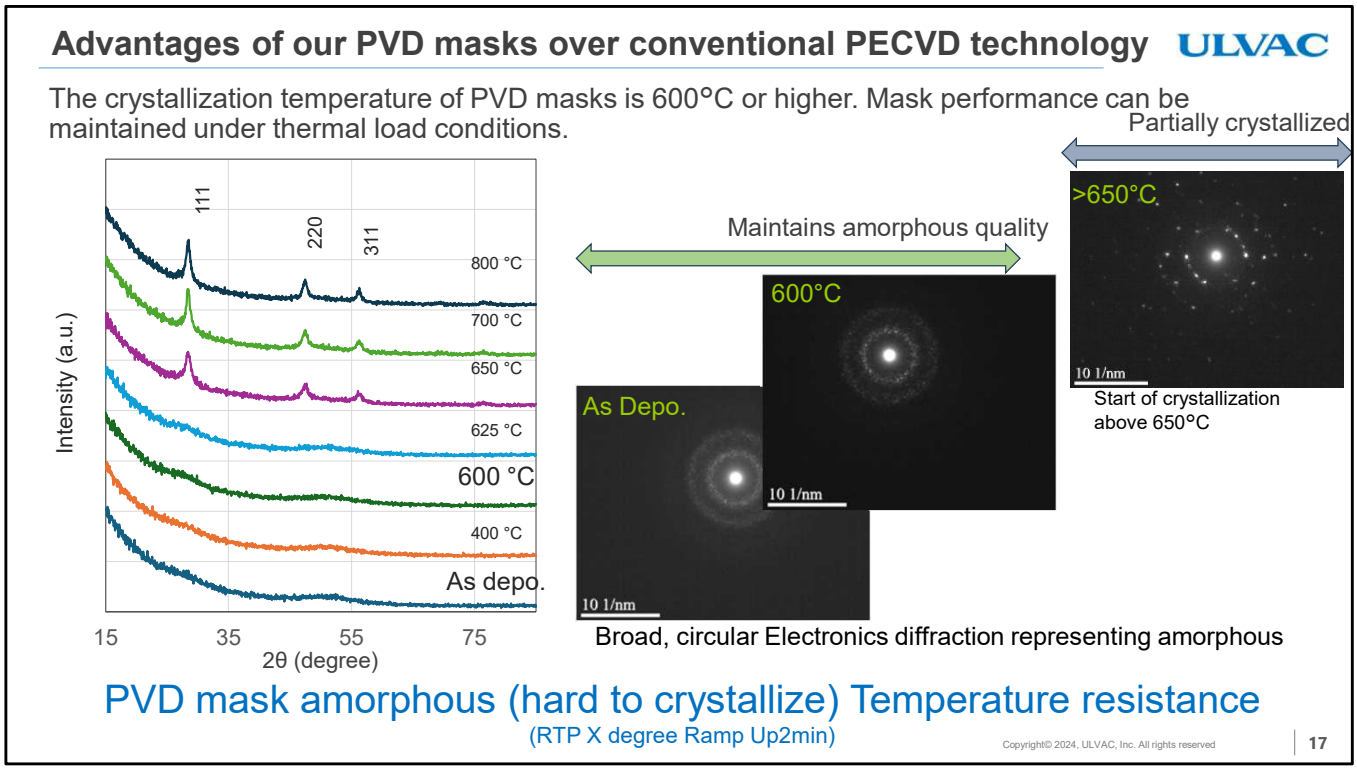
The key technology for any technology is the strength of PVD, low-temperature deposition in an increasingly complex compound process, which reduces the risk of stressing the device structure due to heat load. It also prevents unnecessary diffusion processes from proceeding.

Next, ability to control crystallinity. As I said, it is important to control the film quality to suit the application. High-density, low-resistance film is an important factor for applying PVD films as a substrate. This is important for advanced devices that require low impurity concentrations and reduction of contamination and degassing.



What we will discuss in detail today is the PVD film for the diffusion process.

The diffusion process is a process in which impurity ions are intentionally implanted into silicon to change its characteristics. That is a process which combines the process to implant impurity ions and the heat treatment annealing which recover the crystal defect caused by the ion implantation. It is one of the FEOL and front-end processes that will become even more important in future advanced devices and devices with sheet structures.



In this slide, the superiority of our PVD films in the diffusion process is explained with a schematic device cross-sectional structure.

First are the problems with the conventional technology, or CVD process, shown on the left. The CVD process has advantages in terms of performance and cost, but its problems are also evident in the increasingly complex sheet structure.

Here, the area circled by the blue fan-shaped line is the intended diffusion area as per the targeted design. How will this be maintained? The key question is whether it will be extraordinarily diffused.

First, a conventional technology CVD mask was deposited on the device in orange. Due to the deposition temperature of PECVD itself, there is a risk of unintentional further diffusion of already completed blue, fan-shaped diffusion areas. After diffusion, the diffusion process can be underway. After the diffusion process, there is a problem that the CVD mask crystallizes during the annealing process for crystal lattice recovery and degasification. With further ion implantation, the crystallized mask could begin to lose its shape. The problem of inaccurate diffusion due to misshapen masks is now a major problem in advanced devices.

In contrast, this is the advantage of our PVD masks. Blue PVD mask is deposited. Low sound deposition reduces the risk of unintended diffusion. After diffusion, PVD masks have a property of difficulty in crystallizing during the annealing process to recover the crystal lattice in the diffusion region. In other words [inaudible], the blue PVD mask has the property of not crystallizing.

PVD masks, which are resistant to crystallization, enable accurate diffusion. The diffusion along the blue line is now possible as initially envisioned.

I have explained the importance of being hard to crystallize—or amorphous—film quality as a mask for diffusion. This data shows how our PVD films deposited as masks can maintain amorphous film quality when thermally loaded.

This data shows that the amorphous film quality is maintained in all cases: crystallinity immediately after film deposition, crystallinity when a thermal load of 400°C is applied, and crystallinity when a thermal load of 600°C is applied.

As I mentioned, annealing is always required after the diffusion process to restore the crystal lattice in the diffusion zone, but the data shows that our PVD films have not lost their good properties even under thermal loading.

Problems with conventional technology CVD masks

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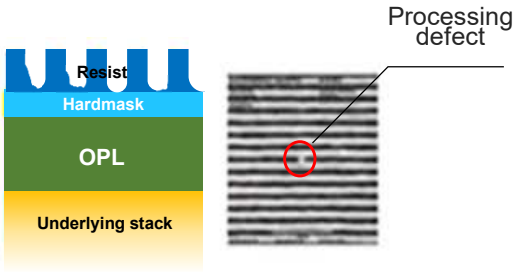
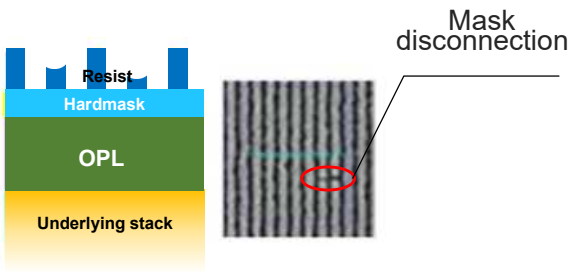
The problem with CVD masks is the adverse effects of released gases on photoresist.

Masks without gas emissions are needed for further miniaturization of sheet structure devices.

1) Due to emitted gas from CVD mask
Photoresist residue, processing defects



2) Due to emitted gas from CVD mask
Collapsed photoresist, processing failure



Source:.
De Silva et al.: Inorganic hardmask development for extreme ultraviolet patterning

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Another advantage of our PVD masks as etching masks is that they release less gas than conventional technology CVD masks.

Conventional mass production technology PECVD masks have advantages in terms of production cost, but there is a risk of the raw material gas emissions caused by chemicals adversely affecting the photoresist. This slide shows two examples where emitted gases adversely affect the photoresist, making them defects.

The first is that the released gas from the CVD mask leaves residue on the photoresist. This leads to processing defects in later processes. Or the photoresist itself is collapsed by the gases released from the CVD hard mask. This is a serious problem that can lead to serious problems such as mask disconnection.

Advantages of our PVD masks over conventional PECVD technology

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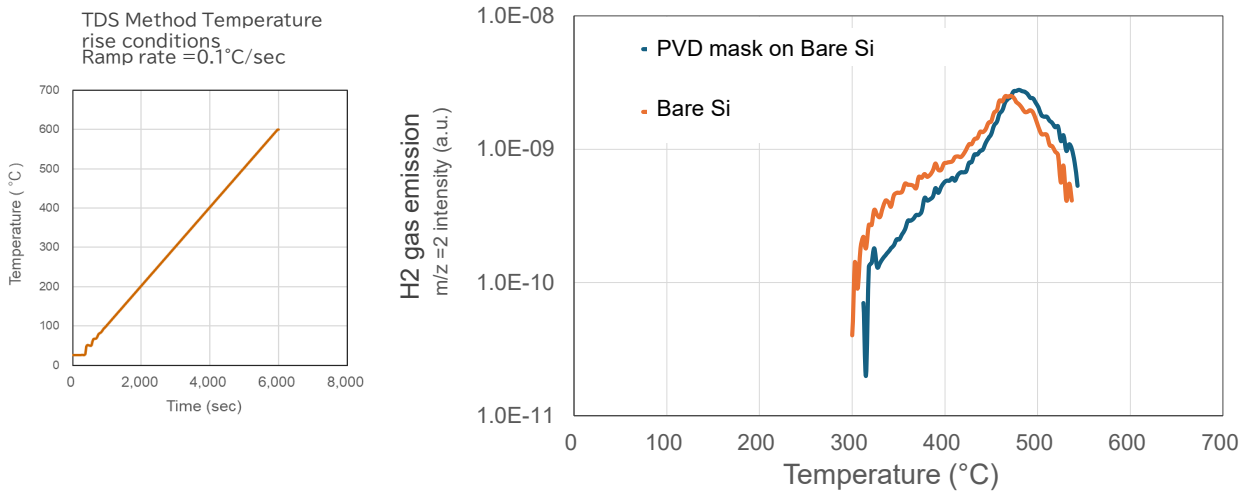
- No emission of H_2 gas that adversely affects photo resist (same level as Bare Si substrates)
- Superior as Etching Mask

Gas emission characteristics in PVD mask As Depo (TDS Ramp rate 0.1°C/sec, max 600°C)



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New masks without emitted gases are needed for the miniaturization of advanced devices.

Shown in this slide is the data that was obtained by measuring the gases emitted from our PVD masks using a technique called TDS. We compared the amount of hydrogen gas released when the temperature was increased for the two wafers under the temperature rise conditions shown on the left: the blue line on the bare silicon wafer deposited by our PVD mask, and the orange line on the bare silicon wafer itself.

The data shows that our PVD masks emit very little gas even without degassing treatment. This film property, together with the PVD mask code, is the advantage of our PVD masks over conventional CVD technology as masks for etching.

1. ULVAC PVD films and their strengths in a complex process
2. Our contribution in memory products for AI and adaptation of hardware
3. New Platform ENTRON-EXX

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Semiconductor Business Progress in Memory Market

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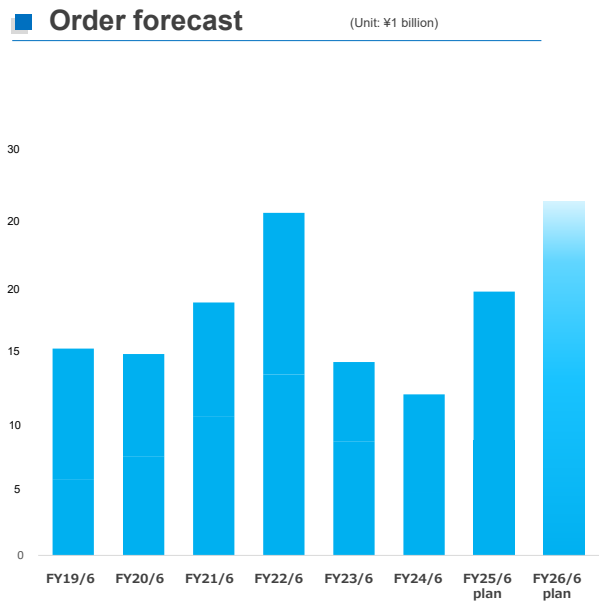

Contribution to BEOL's wiring process

Memory Progress
&
Further growth due to increase in number of customers and processes

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Next, our contribution in memory products for AI chips and the improvements in equipment and hardware technology to be applied to memory for AI chips will be presented.

We have been contributing to memory production with sputtering processes that deposit aluminum, copper, and other wiring materials themselves in the BEOL's wiring processes. In recent years, new business opportunities have emerged along with advances in memory technology.

Advanced AI Chipsets Required Semiconductor Products and Technologies

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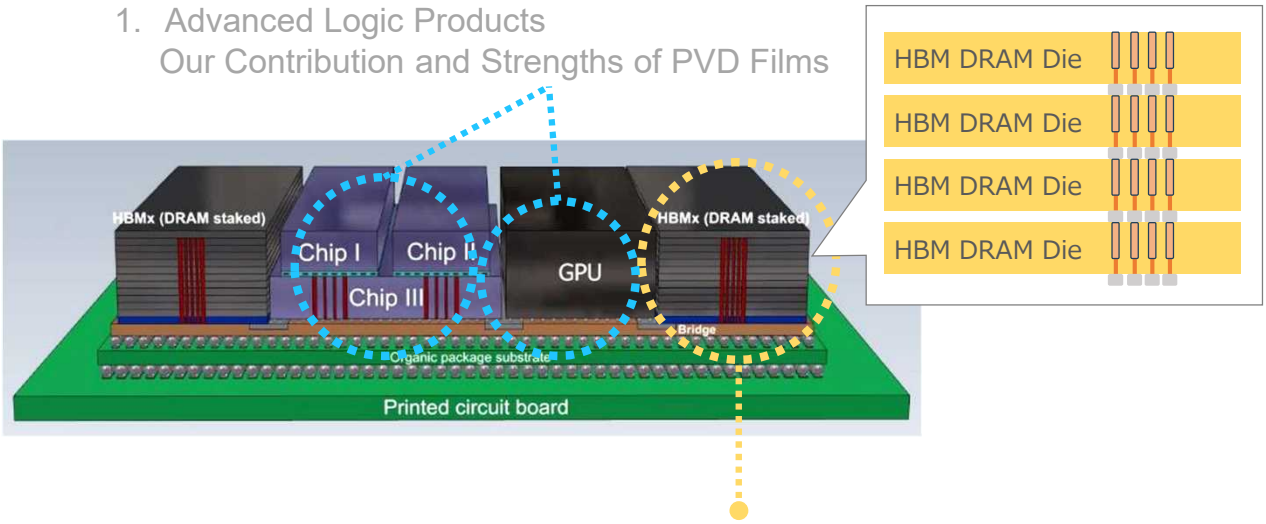
1. Advanced Logic Products
   Our Contribution and Strengths of PVD Films



2. HBM (layered memory) for AI processors
   Our Contributions and Strengths

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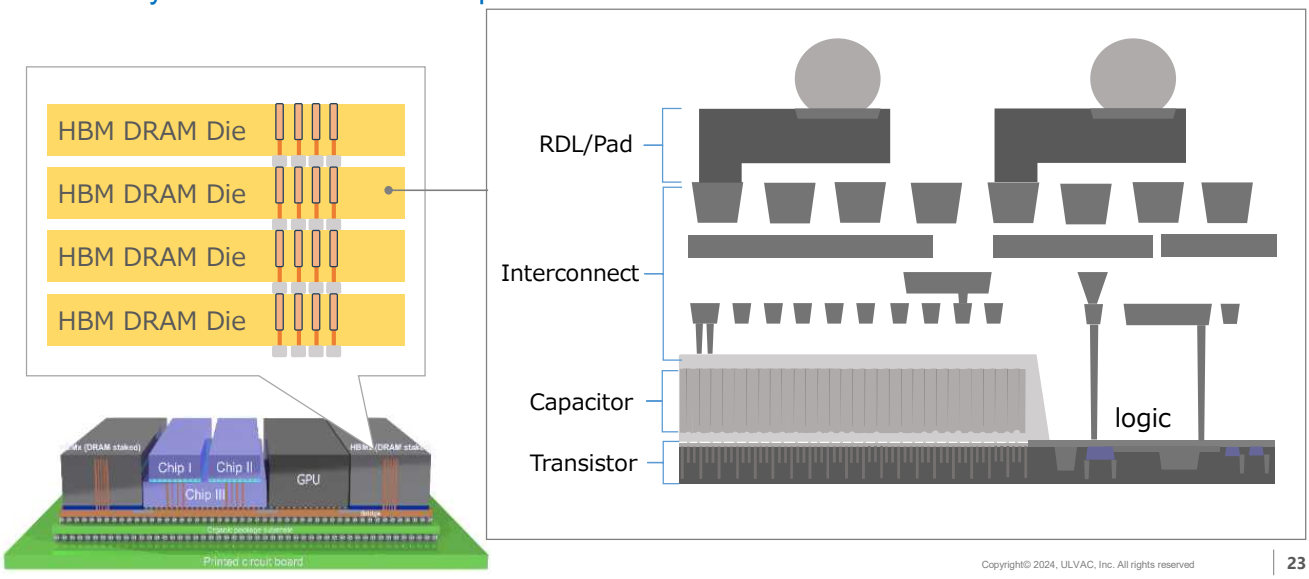
For example, as shown on the slide, our sputtering process is used in the wiring layer that joins DRAM chips together in HBM, the layered memory for AI processors.

Continuous process acquisition and development in Memory (DRAM)

ULVAC

In addition to HBM, process acquisition activities for conventional DRAM (DDR5) are in progress.
⇒Steady increase in number of processes



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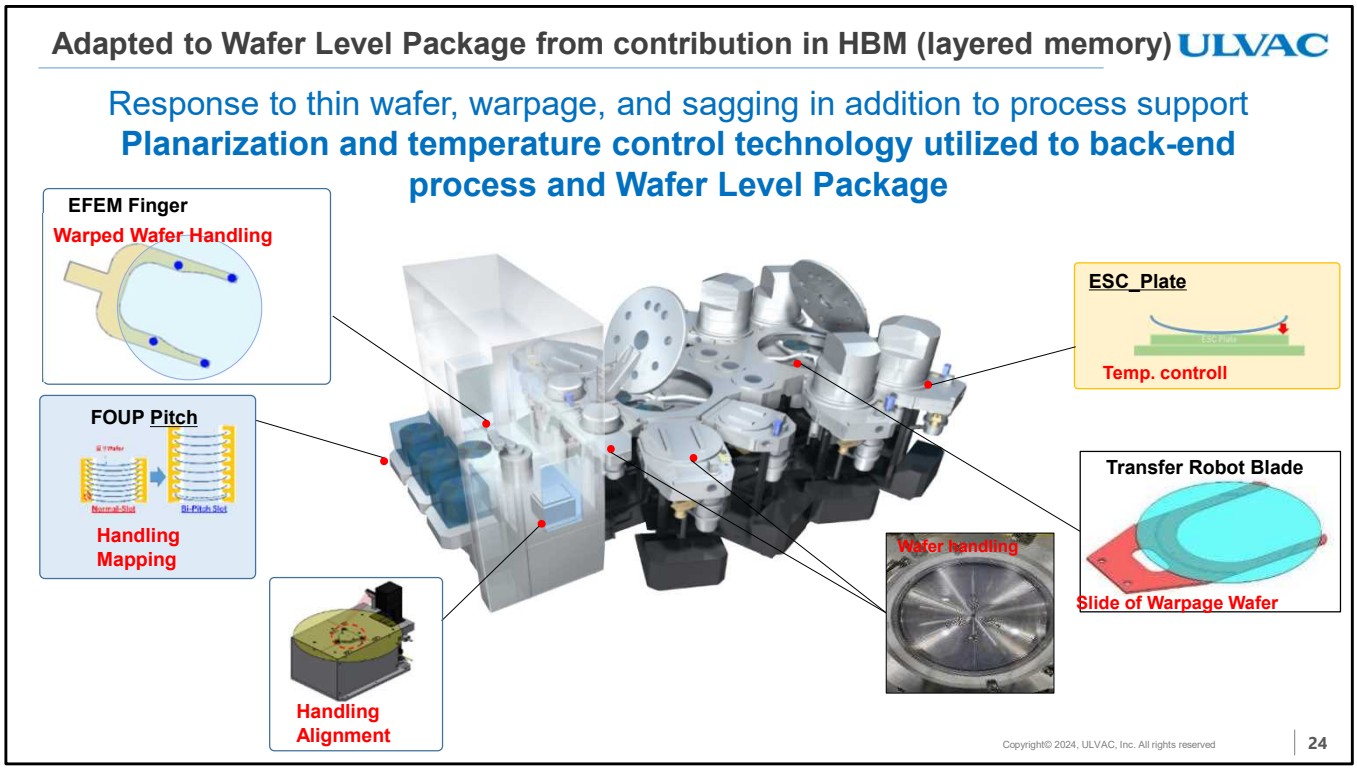
In addition to the interconnecting wiring layer, we also contribute to the change of process from conventional DRAM process to HBM in the DRAM structure shown on the right, and we also apply TiN metal hard masks to memory and contribute to memory products for AI in the process of further miniaturization.



Unlike standard DRAM production equipment, production equipment for HBM stacked memory requires a process that supports wafer flattening and temperature limitation, and hardware that supports warpage and sagging of the wafer. We have worked with our clients to solve unique process and wafer problems.

The process and hardware improvements made here are being utilized in the wafer level package that is currently under development. We also believe that our strength in the field of packaging, with a lineup ranging from cutting-edge device support to large substrate equipment, can be utilized to meet our customers' various wafer level package attempts.

Our support to this packaging will be discussed in detail later in this seminar.

1. ULVAC PVD films and their strengths in a complex process
2. Our contribution in memory products for AI and adaptation of hardware
3. New Platform ENTRON-EXX

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New Equipment

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Equipment name: ENTRON EXX

① Plug-In Platform connection simplification

② Software Extensibility

③ Designed with environmental impact in mind

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Now, I would like to introduce a new device, ENTRON-EXX, which we announced in a press release last week. We have launched a new platform that incorporates our existing process know-how with completely redesigned hardware and software.

This ENTRON-EXX is a new platform with all-new hardware and software that can be installed, including the process introduced today. We have renewed the design, control system, and software of the ENTRON series, which has been renewed repeatedly.

Introduction of new equipment ENTRON-EXX

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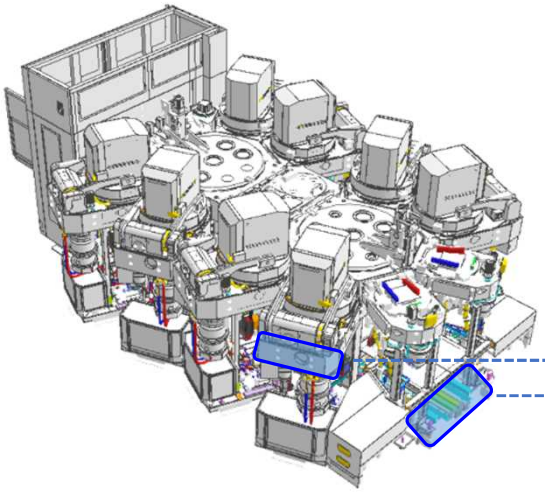
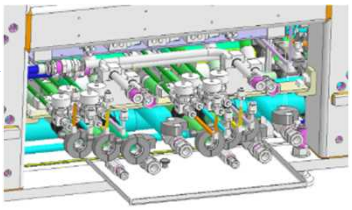
① Plug-In Platform connection simplification

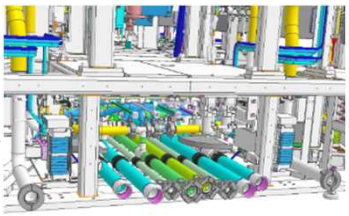
⇒Reduce relocation and remodeling turnaround time by **50%**



☐ Simplified chamber connections



☐ Simplified connection of essential facilities



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Specifically, all utility connections were reviewed and simplified to reduce construction time and manpower requirements. Shortened start-up time and on-site remodeling reduce construction time by 50% from the previous time.

Introduction of new equipment ENTRON-EXX

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② Software Extensibility

Software to support operators

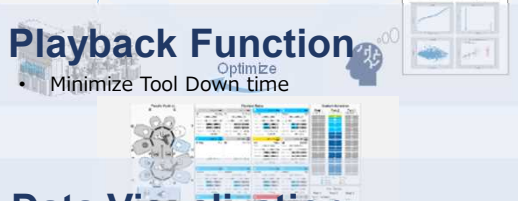
- Prevent human error (Parameter, Recipe)

AI

- Process parameter Optimization

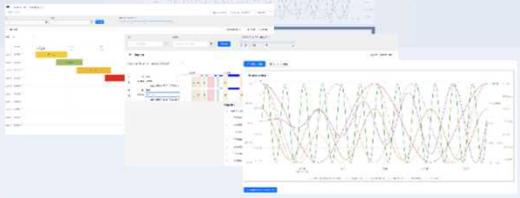
Playback Function

- Minimize Tool Down time



Data Visualization

- Tool Healthy monitoring



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Newly designed software comes with more user-friendly functions and analysis tools. It includes process recipes with AI tools, pre-checking of parameters, a playback function to help operators reproduce past troubles on the equipment, and pre-monitoring to determine if what just happened is abnormal or normal compared to last week's process or last month's process.

Introduction of new equipment ENTRON-EXX

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③ Sustainability

Designed with environmental impact in mind

- **20%** reduction in power consumption in standby mode
- **Up to 10%** reduction of installed floor space in clean rooms
- Regular maintenance consumables are fully compatible with conventional models
- Sputtering target recycling program under consideration

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The new machine is designed with both sustainability and environmental impact in mind, with 20% less power consumption and 5% to 10% less floor space in clean room than conventional machines. More details will be provided at this week's SEMICON Japan.

As mentioned above, we are currently executing activities to increase our market share with our process, equipment, hardware, and our new platform ENTRON-EXX.

Technology Center

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Technology Center PYEONGTAEK, Pyeongtaek, Korea

Opening Ceremony

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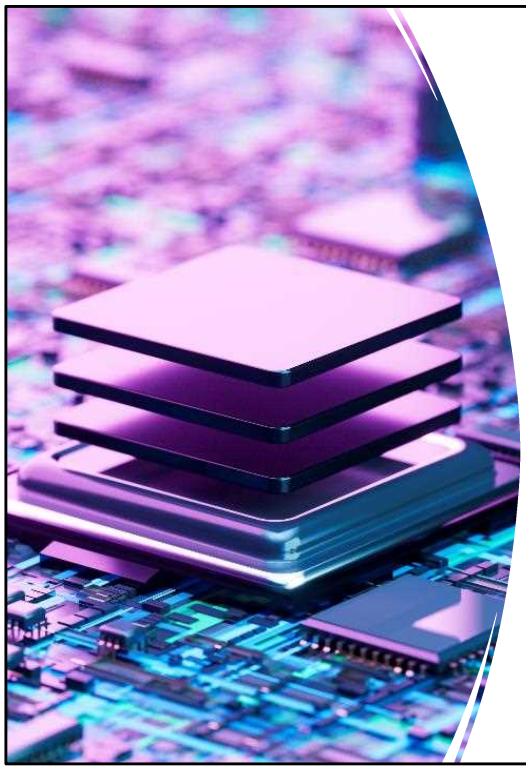
We also opened a technology center in Korea to speed up development and further strengthen R&D.

We are increasing joint development with our customers and aggressively investing in what will lead to business expansion quickly after development.



State of Advanced Packaging and Our Approach

Executive Officer, General Manager of Advanced Electronics Equipment Division, Equipment Business HQ
Harunori Iwai
Business Planning Department, Advanced Electronics Equipment Division, Equipment Business HQ
Junya Kubo

I am Iwai from the Advanced Electronic Equipment Division. Now, I and Kubo will explain the current status of advanced packaging and our company's efforts in this area.

1. About Advanced Packaging
2. Interposer and Descum processing
3. Panel Level Packaging and Our Surrounding Environment

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First, let me talk about the advanced packaging.

Elements required for AI semiconductors

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- Semiconductor miniaturization
- Adoption to HBM
- Application of new materials
- Application of new structure

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We have described the elements required for AI semiconductors. While logic, the miniaturization of memory, the support to HBM, new materials and new structures that Iwasawa is working on are more important than ever, packaging technology is currently evolving as well.

Role of Advanced Packaging and Evolution of Technology

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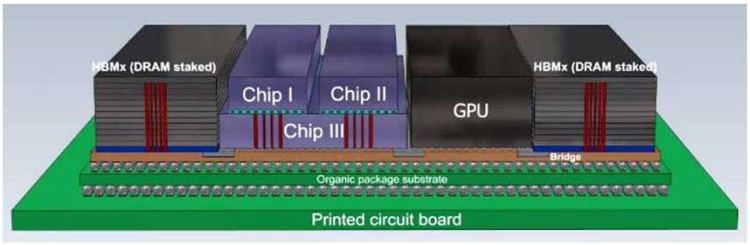
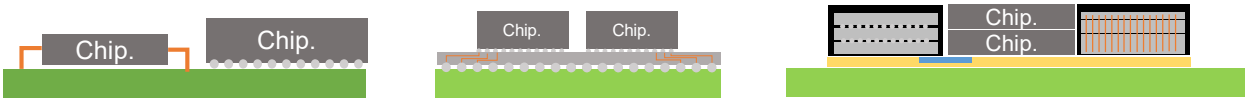
Role of Packaging (fine, short, high-density connection of wiring)



Evolution of Packaging Technology

Existing Packaging	Advanced Packaging	
✓ Lay out individual chips	✓ Multiple chips side by side on the same substrate →Short and dense wiring	✓ Mounting Chips directly on the chip →More memory in multiple stages ✓ Use materials other than Si such as resin, glass, etc.



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One of the elements required for packaging is the need to make transfer data between the memory and the processor faster in order to process large amounts of data. It must handle more wires in the same area and achieve high efficiency and high reliability.

Various new materials and structures are being investigated and developed in combination to make wiring thinner, shorter, and denser.

In AI semiconductors, dedicated chips are being created for many applications. In the past, individual chips were arranged in a row, but challenges to various structures are continuing in order to achieve power consumption, high efficiency, and high reliability at high speeds.

The use of multiple chips side-by-side on the same substrate is being considered for shorter wiring and higher density, and for even higher density and efficiency, mounting chips directly on the chip or using silicon substrate materials such as resin and glass is also being considered.

Our technologies used in advanced semiconductor packaging

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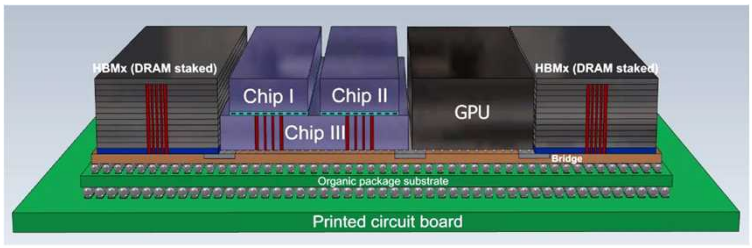

- Plasma Dicing
- TSV etching (through-silicon substrate processing)
- Etching for glass processing (optical waveguide formation)
- TGV Glass substrate hole etching
- Etching for microfine patterning
- Plasma surface activation (hybrid bonding)
- Electrode formation sputtering
- Seed sputtering for packaging substrates
- Desmear treatment for packaging substrates
- Descuming for interposer

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I am Kubo of the Advanced Electronic Equipment Division, Business Planning Department.

In the area of AI semiconductor manufacturing, the manufacturing process is becoming increasingly complex. This has led to an increase in the use of vacuum technology for processing with higher precision. In the packaging area, our sputtering, etching, and descum technologies, which use vacuum equipment and plasma technology as a base, are compatible with many advanced packaging technologies.

Today, we would like to introduce our approach to processing equipment for new materials, which are particularly characteristic of advanced semiconductor manufacturing.

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I am Kubo, Business Planning Department, Electronics Division.

Now, let us explain the interposer and Descum process.

What is an interposer?

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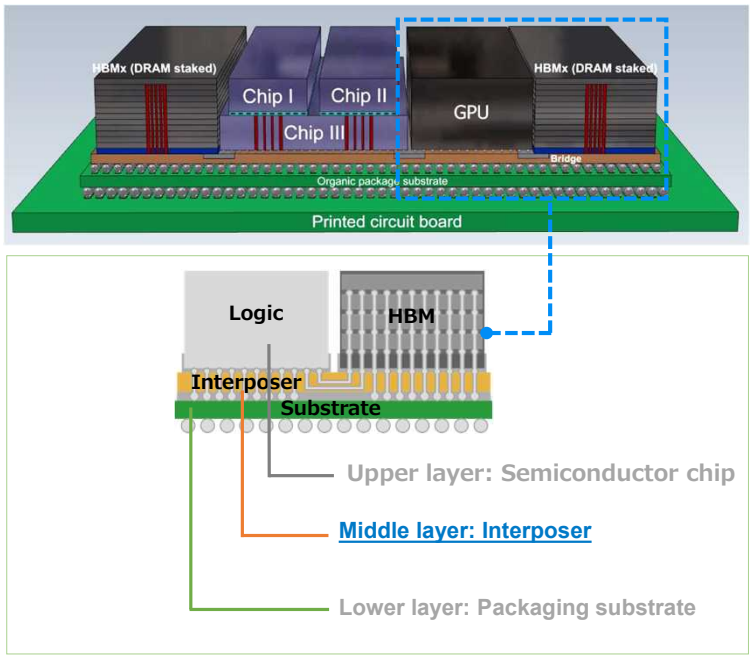

Interposer Functions

- Streamlining Connections
- Space Savings
- Signal quality improvement
- Improved thermal management

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An interposer substrate is a special board that successfully connects small electronic components such as semiconductors. This board allows the latest semiconductors to exchange information with each other very quickly.

This interposer substrate has several useful features. By connecting many chips efficiently, the entire machine can be made smaller. It also shortens the distance over which information is transmitted to ensure that it is delivered properly. Furthermore, by allowing the heat to escape successfully, the entire package does not get too hot and can be made to last longer in a stable manner.

Thanks to these features, interposer substrates help create high-performance, reliable AI semiconductors.

Interposer Technology Trends

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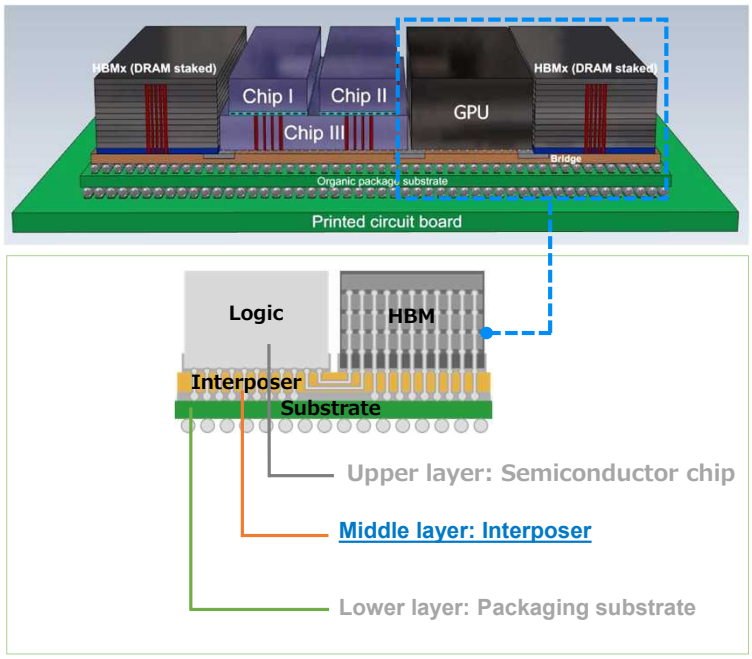

Interposer materials

Miniaturization technology

Silicon + Si substrate

Resin

Diverse Approaches

utilizing the characteristics of resin and silicon

Resin ✖ Silicon Si substrate

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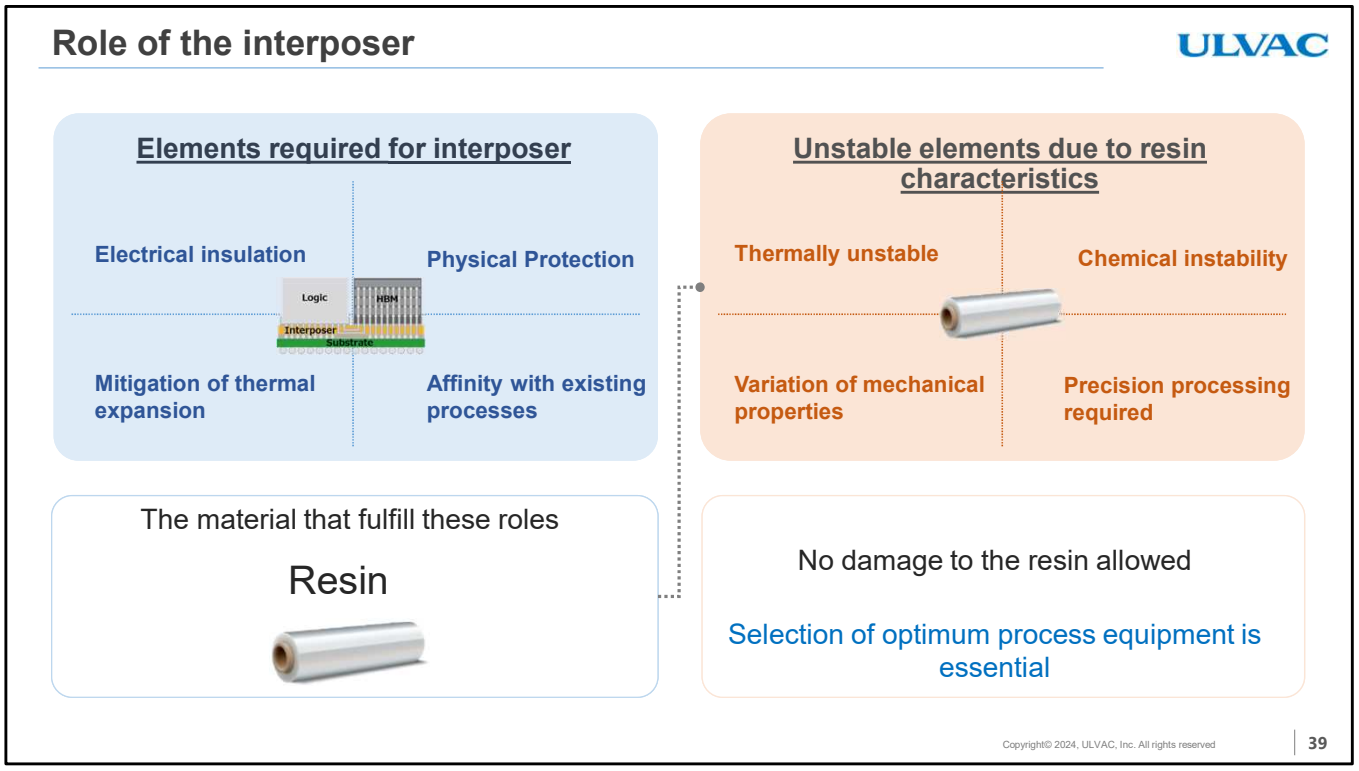
Interposer technology in semiconductor packaging has evolved significantly in recent years. Specifically, advanced packaging combining silicon substrates and resin improves packaging performance through miniaturization technology based on silicon device fabrication technology.

There is also a shift toward interposers that use resin as the substrate material. Benefits include reduced manufacturing costs and design flexibility for resin interposers. This has led to the search for a variety of approaches that take advantage of the properties of resin and silicon to provide optimal solutions for specific applications.



These technological advancements, selected for different applications and performance requirements, play an important role in supporting technological innovation in the semiconductor industry.

There are several important requirements for interposer substrates. First, it must have the function of electrical insulation. This is to ensure that different electrical circuits do not short-circuit and are safe and reliable. Next, physical protection is required. This is to make the device more resistant to external shocks and vibrations so that it is less likely to break.

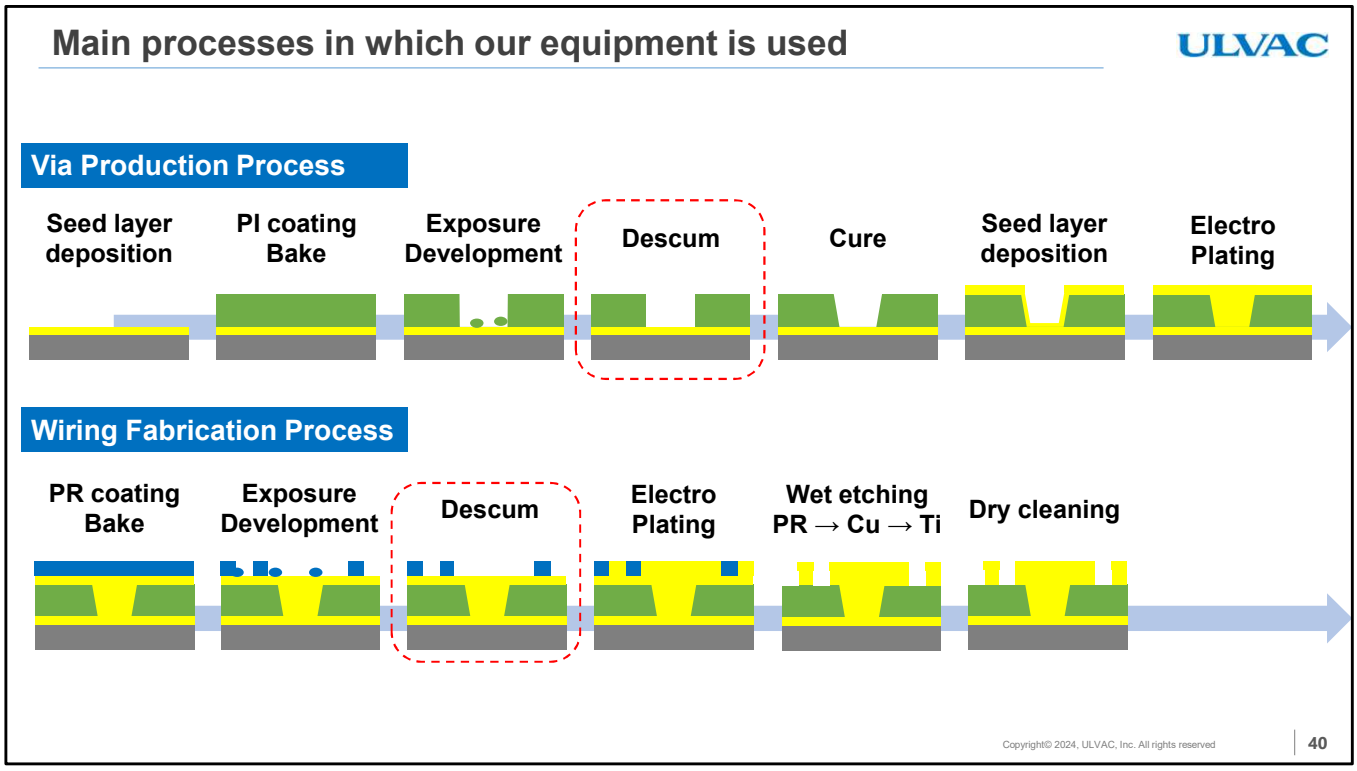
Mitigation of thermal expansion is also important. This is to reduce the stress caused by temperature changes by adjusting the degree to which different materials swell at different temperatures. In addition, affinity with existing manufacturing processes is also needed. This is to get in between the various devices and make it easier for materials to stick together and create shapes to make manufacturing more efficient.

A variety of resins are used to meet these requirements. Resin is a key component of interposer performance and reliability. Resin has many convenient points, but there are a few things to keep in mind.

First, it has the property of being sensitive to temperature. Resin is easily reshaped by heat, so equipment that controls temperatures well is necessary. Second, it is chemically less stable. Resins can react with other substances and change, so the equipment should be designed with this in mind.

There is also variation of mechanical properties. Resin is not very strong and must be handled gently to avoid breakage. Finally, precision processing is required. When using resins, there is a lot of fine work to be done, so careful processing equipment is needed.

Considering these properties, it is important to select the best process equipment for processing resins.

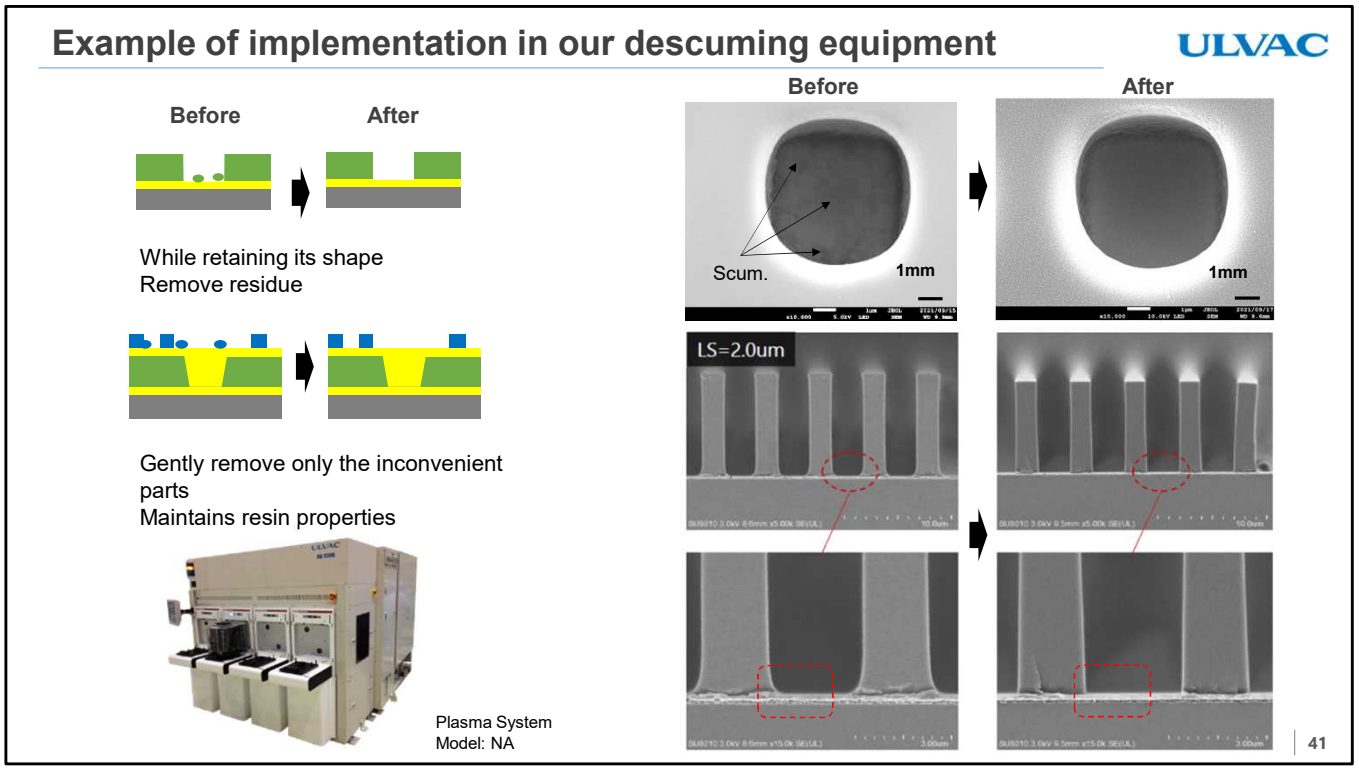


Interposer fabrication involves a process called descum, which cleans off the residue after the resin is processed.

Here is an explanation of the upper processes in the slide. There is something called Via made on the substrate to electrically connect the semiconductor components.

In making this Via, holes are drilled in a type of resin called polyimide to form it. However, this process may leave an unremovable residue at the bottom of the hole after it is drilled. It is important to remove this residue. Since all holes must have the same electrical properties, only the residue must be removed without changing the size of the holes.

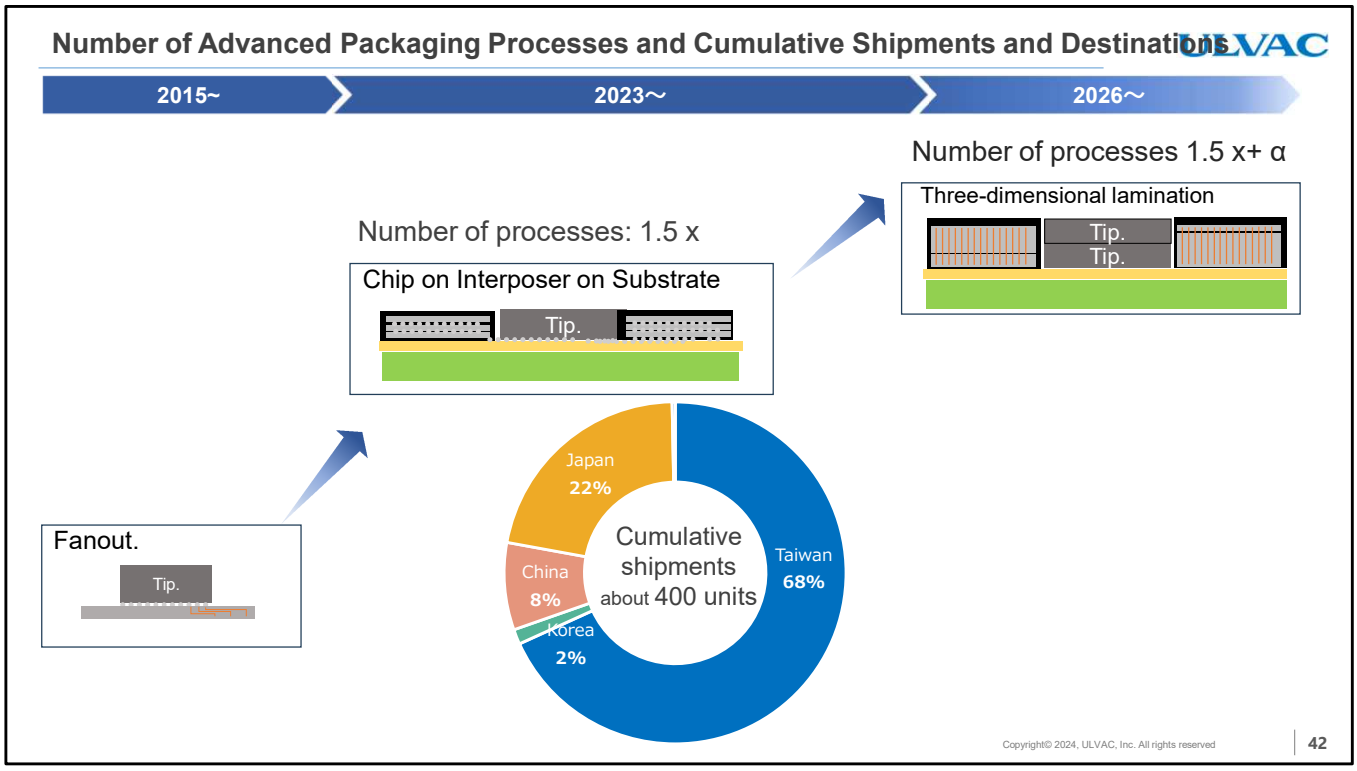
The wiring fabrication process also involves the removal of residues. In the example of the lower processes of the slide, the residue must be removed without changing the shape after processing into a resin called photoresist.



To remove the residue, a process called descum, which uses plasma technology, contributes.

The photo above shows an example of via residue removed. The diameter of the hole is about 5 micrometers, which is about one-tenth the thickness of a hair. It is required to remove the residue from the bottom of the hole while gently handling it so as not to break the hole. If you look at the shape of the shaft, you will notice that the resin shape has not changed, but the discoloration at the bottom has been cleaned up.

The photo below shows an example of residue taken from between two micron-meter resin columns. This is an even finer line than the 5-micrometer hole mentioned earlier. Only the inconvenient parts are gently removed while maintaining the characteristics of the resin. Our descum equipment achieves gentle processing for resins in miniaturized working processes through a unique configuration that combines microwave plasma technology and parallel plate plasma technology.



In addition to wafer processes, unique transfer systems and process quality configurations that can transfer dicing frames can also be selected to handle segmented chips.
Our technology has enabled more complex packaging configurations, contributing to the AI semiconductor packaging market.

This equipment consists of several options, which include metal etching, surface treatment capability, as well as descum processing to wafers. As for the transport system, it can handle not only wafers but also dicing frames, which enables the system to accommodate customers' special manufacturing methods. In addition, throughput is 1.5 times that of the competitor, contributing to increased productivity.

Compared to conventional packaging for smartphones, AI semiconductor packaging is expected to require more than 1.5 times the number of processes, and the number of equipment shipments is expected to be the same. In the future, an increase in the total number of packaging is always under consideration, not only to further increase the number of processes, but also to study the application of hybrid bonding for 3DICs and HBM 3D lamination, which are being considered for inclusion in the future.

The evolution of packaging technology has created new processes that have never existed before, creating business opportunities for our company. About 70% of equipment is destined for Taiwan. As you know, the packaging business continues to expand and grow from Taiwan to the rest of the world, and this growth is expected to continue.

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I will continue with an explanation of our response to the expansion of packaging substrates and interposer substrates.

Technology Trends in Packaging Substrates

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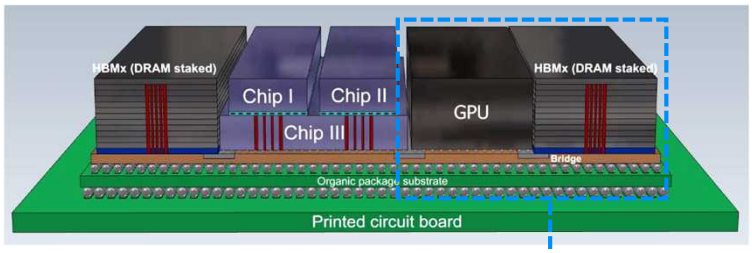

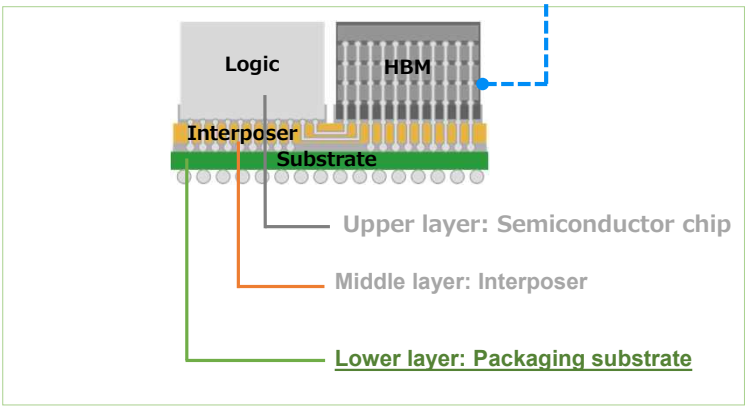

Challenges in packaging substrates

Resin

WET process ⇒ DRY process

Resin ➡ Glass

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The expansion of packaging substrates and interposer substrates is being considered to further integrate multiple semiconductors in a single package to achieve higher performance and multifunctionality. Packaging substrates, in particular, have been made using the wet process, but the dry process, or vacuum technology, is being considered for further miniaturization.

In addition, packaging substrates are currently mainly made of resin, but glass materials with properties that are suitable for the demands of packaging technology are being considered.

Contribution to PLP (Panel Level Packaging) process

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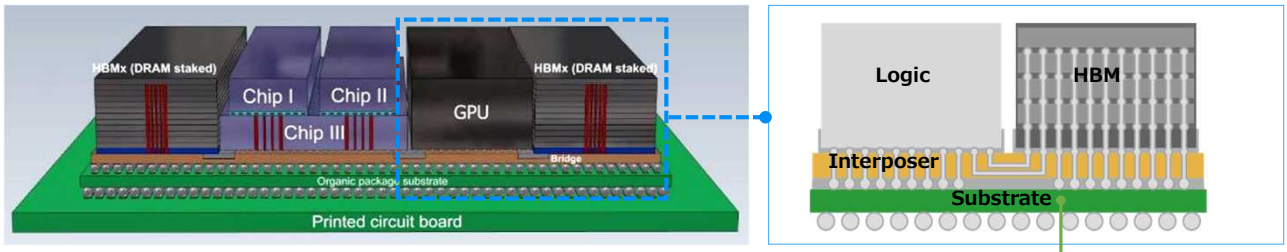
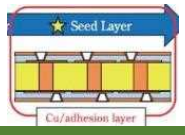
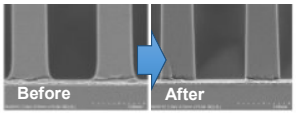


■ **Electrode formation for panel**
» Formation of metal thin film for electrode on large size substrate



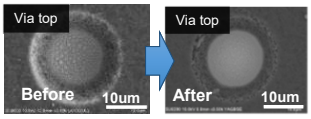
Packaging Substrate

■ **Descum**
» Residue removal after litho of photosensitive materials



Large Interposer

■ **Desmear**
» Removal of residue after laser processing



Packaging Substrate

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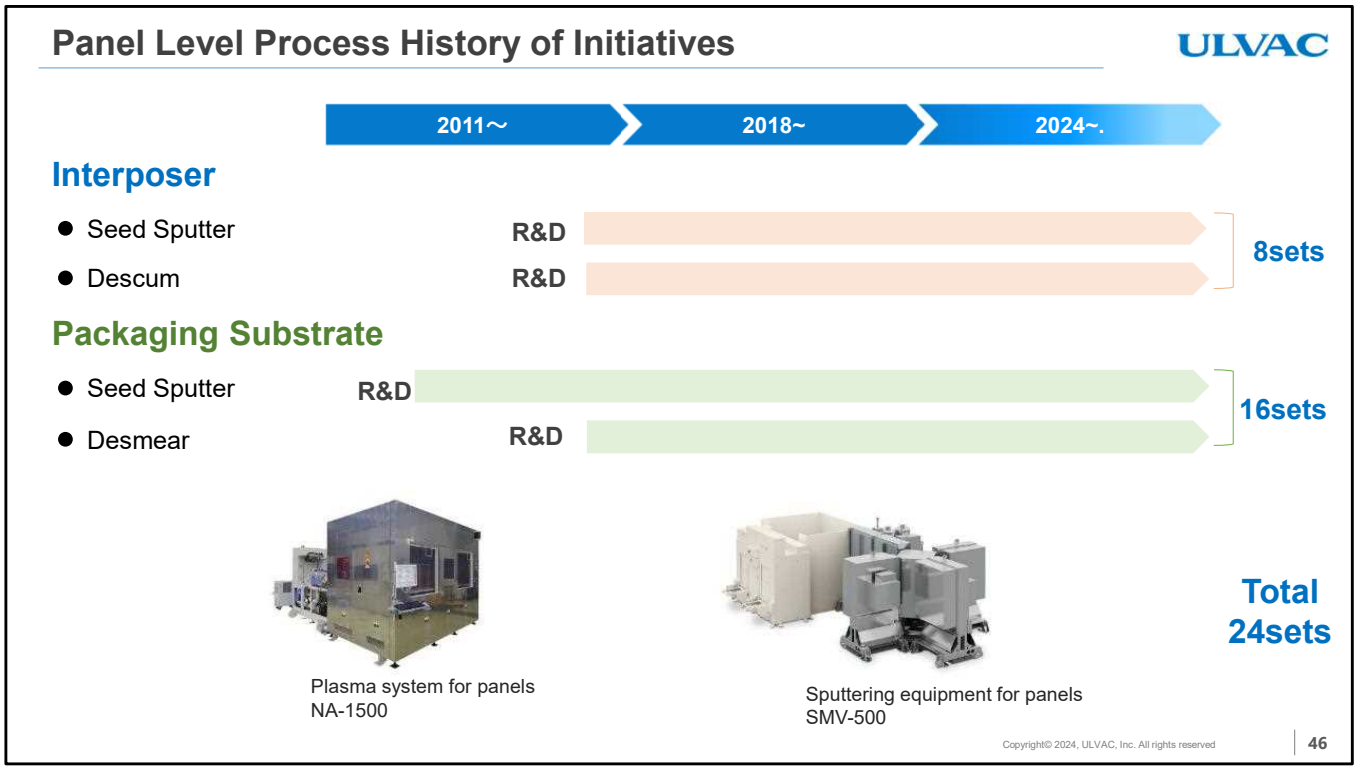
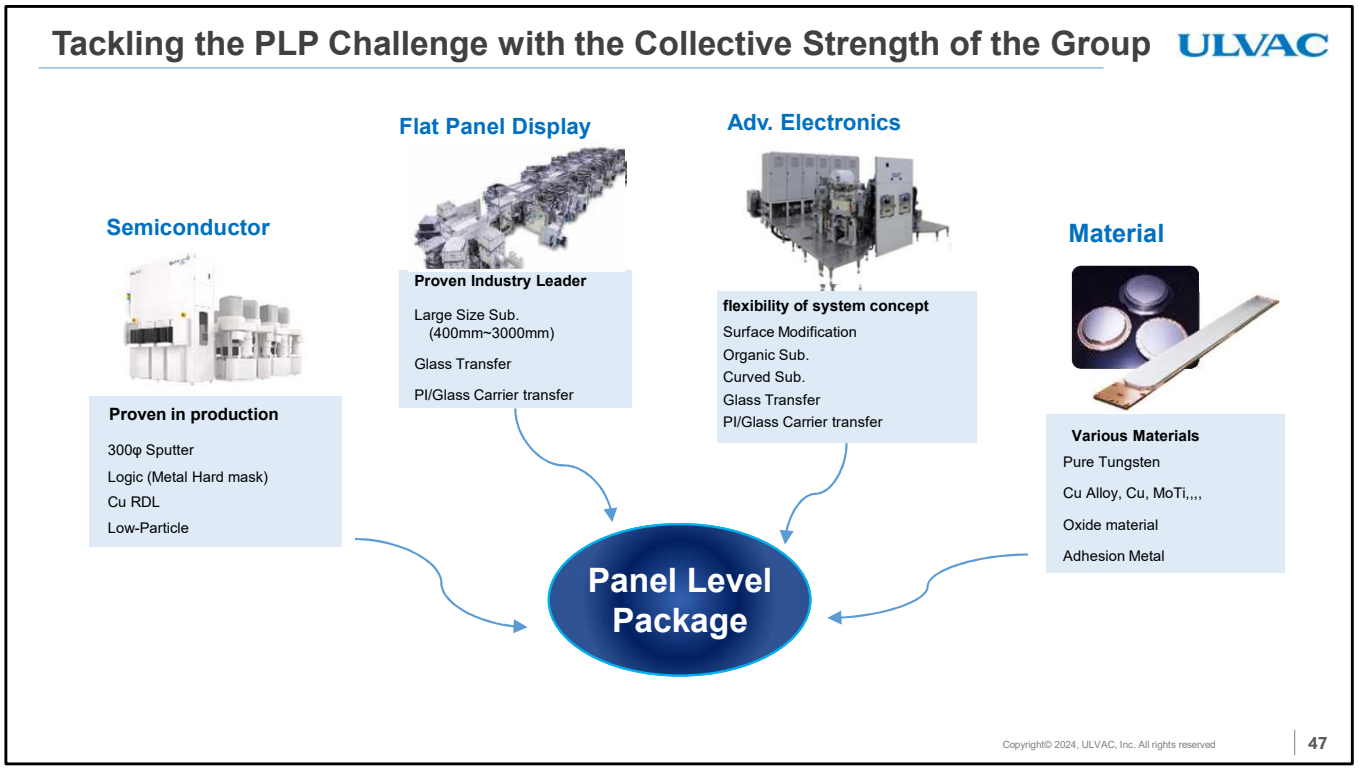
In panel level packaging, where larger panel size substrates are used for packaging, in addition to the descum process introduced so far, we can contribute with desmear equipment for removing and smoothing silica, etc. remaining on the inner wall, and sputtering equipment for seeding to form electrodes using our display manufacturing equipment technology we have cultivated over the years.



We have been working on panel level development since 2011, and have changed substrate sizes and the shape of our equipment as devices have evolved. The NA-1500 plasma system for panels and the SMV-500 sputtering equipment for panels are used to manufacture packaging substrates.

Since the release of the equipment in 2011, we have been working with various companies on R&D-based collaborations to address a variety of issues. The knowledge gained while conducting these activities has allowed us to continue to improve our equipment in response to market conditions, and we have now delivered more than 20 units to panel level packaging manufacturers.



In the field of packaging substrates, square 500-mm and square 600-mm size resin and glass are used as base materials. We have a wide variety of technologies and are capable of developing all kinds of equipment using these technologies.

The Company possesses semiconductor-level technology that can handle the ongoing miniaturization, and has a high share of the equipment market for flat panel displays, excelling in the handling of large glass substrates.

Our advanced electronic equipment division specializes in meeting customer requirements by incorporating semiconductor and flat panel display equipment technologies for a wide variety of applications. The materials division handles a wide variety of materials and can propose target shapes and specifications to suit the equipment.

Also combining the knowledge of our advanced laboratory with specialized experiences, the entire company is working together to provide efficient solutions.

Packaging-related consortiums

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Participation in US-JOINT, a consortium of 10 Japanese and U.S. companies in materials, equipment, etc., established in July 2024

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In the packaging field, companies and engineers from adjacent processes are actively interacting with each other. Prompt communication is required to solve new problems that arise every day in new ways.

We have also joined Resonac's consortium called US-JOINT and have begun activities to incorporate US technology trends. This enables technology development from a global perspective and early exposure to the latest packaging technology conceived by fabless companies for use in equipment development. Through this cooperation we can accelerate the development of new technologies.

Expand growth of Semiconductor & Packaging business

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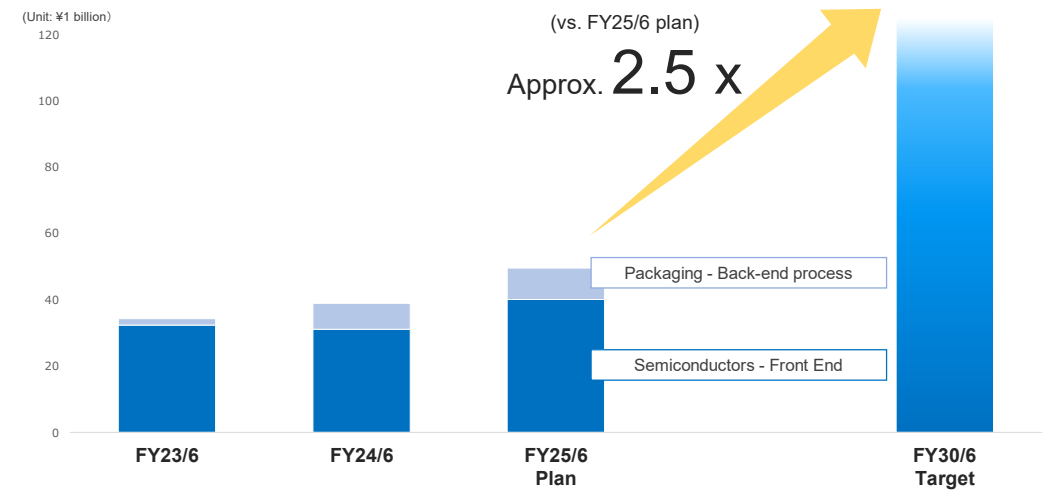

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So far, we have explained our efforts related to interposer substrates, which are an important technology in our semiconductor packaging, and panel level packaging, for which businesses are expected in the future.

In the logic and memory front-end processes that Iwasawa is working on, we aim to nearly double its semiconductor business from the current order size by around 2030. On the other hand, in the back-end packaging business, which Kubo and I are working on, we aim to expand orders nearly fourfold from the current scale by around 2030.

Both of these targets exceed the projected growth rate of the semiconductor market, and we will focus on expanding our business to 2.5 times the scale of our logic and memory semiconductor and packaging businesses combined.

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