

## ULVAC IR Seminar 2025

### Aiming for Further Growth in the Semiconductors and Electronics Field

October 3, 2025

#### Disclaimer regarding forward-looking statements etc.

- **Forward-looking statements**

Forward-looking statements of the company in this presentation are based on information that was available at the time these documents were prepared. There are several factors that directly or indirectly impact the company performance, such as the global economy; market conditions for FPDs, semiconductor, electronic devices, and raw Materials; trends in capital expenditures and fluctuations in exchange rates. Please note that actual business results may differ significantly from these forecasts and future projections.

- **About This Document**

Please note that this IR seminar material and presentation were not created for technical purposes and contain simplifications to facilitate investor understanding.

## Growth Strategy

### Selection and concentration of a business portfolio centered on semiconductors and electronics

- Accelerate focus on Semiconductors and Electronics
- Create new semiconductors and electronics-related businesses by leveraging synergies among businesses
- Expand business through M&A and other initiatives

Approx. **¥110 billion** increase



Consolidated net sales improvement by FY31/6

In August, we announced a new mid- to long-term management plan.

As part of our growth strategy, we are focusing and concentrating our business portfolio mainly on the semiconductors and electronics fields.

We aim to accelerate our focus on the semiconductors and electronics sector and create new semiconductor-related businesses by leveraging synergies across our businesses, driving further growth.

Today, we will introduce our initiatives in semiconductors and electronics, as well as our efforts related to surface analysis systems, as part of our semiconductor-related business.

## Today's Agenda

- 1 Initiatives for Semiconductor Process Expansion**  
16:05-16:20  
Tomoyasu Kondo, Senior Executive Officer,  
General Manager of Semiconductor Equipment BU
- 2 New Initiatives in Advanced Packaging**  
16:20-16:35  
Harunori Iwai, Senior Executive Officer  
Junya Kubo, Sales Department 2  
Semiconductor and Advanced Electronics Business HQ
- 3 Strengths of the Surface Analysis System and Future Developments**  
16:35-16:50  
Hirohisa Takahashi, Executive Officer,  
President and CEO of ULVAC-PHI, Inc.  
Takuya Miyayama, Senior Manager,  
Product Strategy Department, ULVAC-PHI, Inc.
- 4 Q&A**  
16:50-17:10

# Initiatives for Semiconductor Process Expansion

Tomoyasu Kondo  
Senior Executive Officer,  
General Manager of Semiconductor Equipment BU



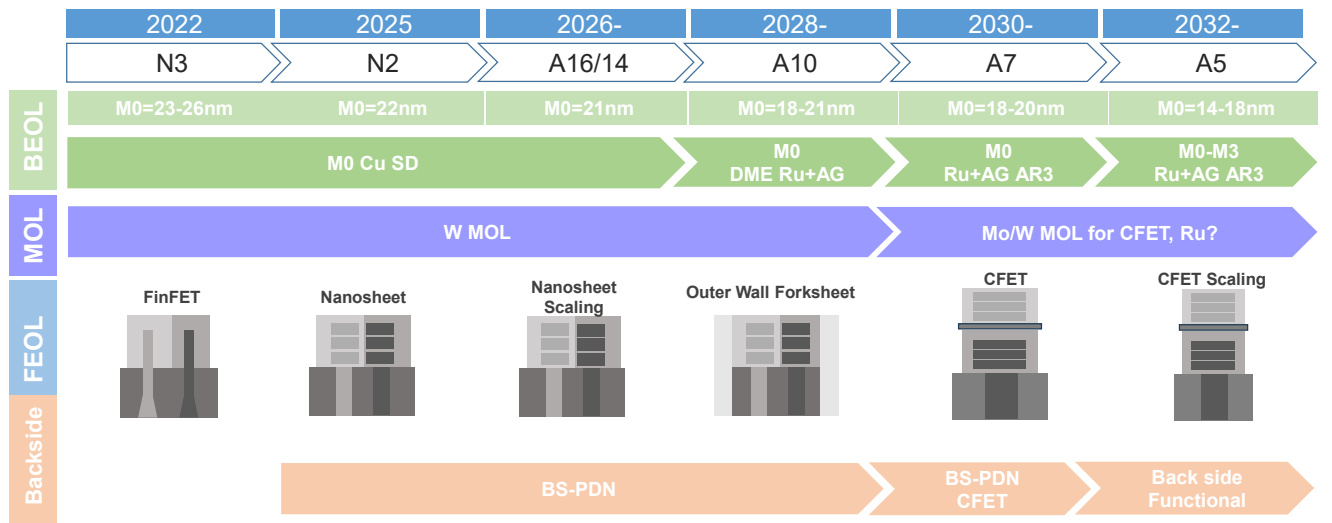
ULVAC

I'm Kondo, Head of the Semiconductor Business Unit.

Today, I will introduce our efforts in the front-end semiconductor process area as part of ULVAC's growth strategy.

# Advanced Logic Foundry Technology Roadmap

- > New Mid-to-Long-Term Management Plan Over the six years through FY31/6, the significant structural changes to semiconductor devices will occur
- > Increased patterning steps and adoption of new materials will expand opportunities for our core PVD deposition processes



Source: Created based on Imec Roadmap

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As you know, semiconductor devices have evolved mainly through miniaturization over the years.

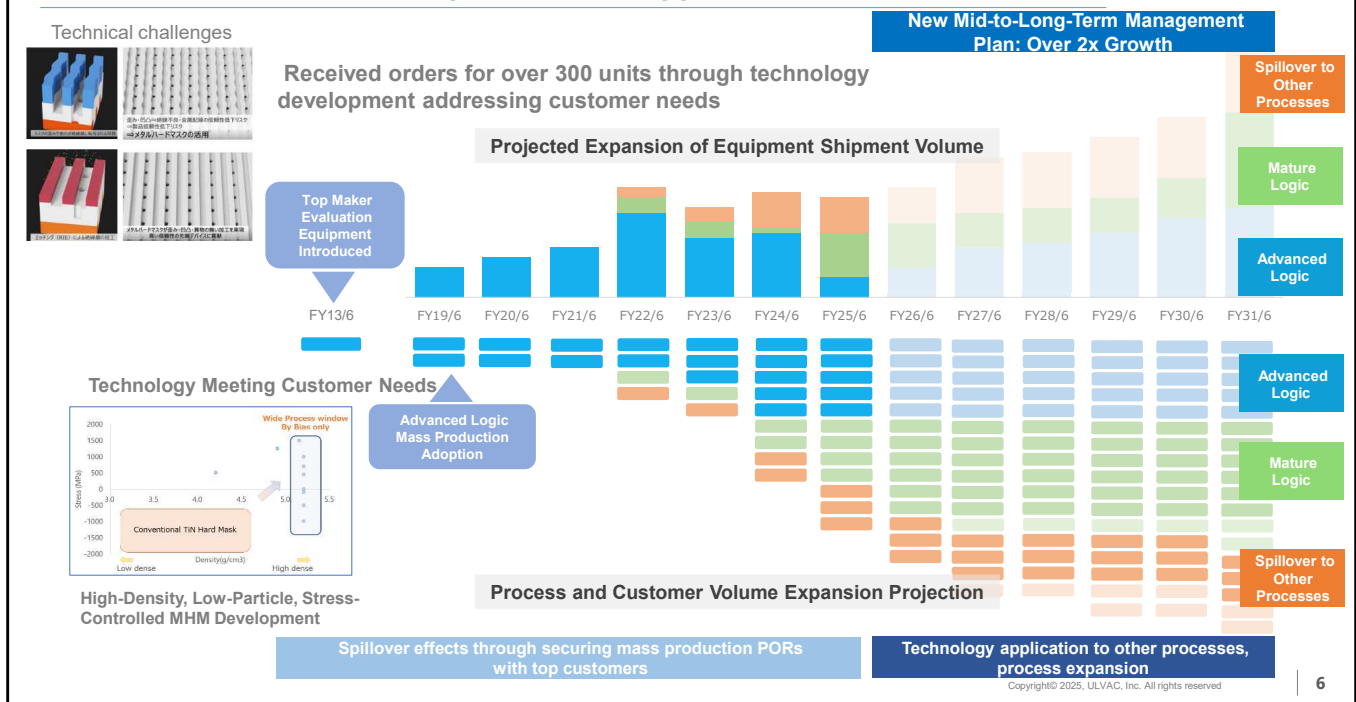
Recently, changes in transistor structures and developments to utilize the wafer backside have accelerated, with some structural changes already realized in leading-edge devices.

As shown here, the recent transition is from FinFET to GAA (Gate-All-Around), along with backside power supply.

Looking ahead to the next six years through FY31/6, further structural and material changes will occur.

In response to these changes, such as increased patterning steps and adoption of new materials, we see new opportunities in our core PVD (Physical Vapor Deposition) field and therefore strengthening our development activities.

# Our Hard Mask Process Expansion and Application to Other Processes



This image illustrates the development and mass production adoption of our TiN MHM process, a field where we excel.

MHM (Metal Hard Mask) is a process to realize fine-pitch wiring, as shown in the top-left diagram. Its superior performance is shown in the graph below, where the vertical axis is film stress and the horizontal axis is film density. Conventional TiN MHM deposition technology was limited to low-density compressive stress regions, but we have achieved a wide range of deposition performance from tensile to compressive stress at high density.

The upper bar graph shows the number of units delivered, and the lower bar graph shows the number of PORs (Proof of Record). This indicates expansion from leading-edge to mature nodes and application to other processes.

In 2012, we started development and evaluation with a major logic foundry to solve their technical challenges, achieving technology development that met customer needs, leading to mass production adoption in 2018 (5nm generation) after about six years.

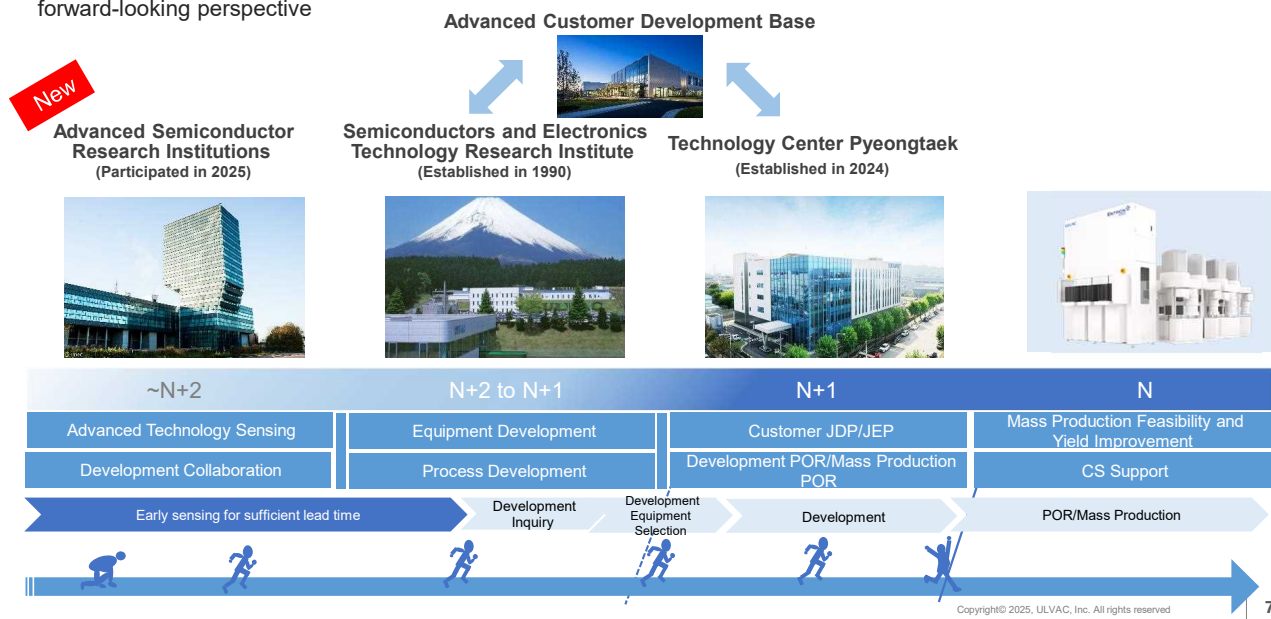
Leveraging this achievement, we have won mass production adoption with other major logic manufacturers and mature logic foundries including those in China. We continue to gain PORs by applying this technology to new processes.

We aim to sell over 300 ENTRON HM systems by FY31/6.

Reproducing such success stories is crucial to enhancing ULVAC's value, and we are intensifying our efforts to achieve this.

# Our Advanced Semiconductor Development Framework

- Strengthening Advanced Semiconductor Device Development: In addition to opening the Technology Center Pyeongtaek (Korea), we have commenced participation in the Imec program in Belgium. We are building a development framework with a forward-looking perspective



Now, let me explain our development system to achieve value enhancement.

First, the most important is our N+1 development with customers (N=current generation, N+1=next generation, N+2=subsequent generation).

We actively conduct joint development and evaluation using two sites: the Technology Center in Pyeongtaek, South Korea opened last year, and customer development lines.

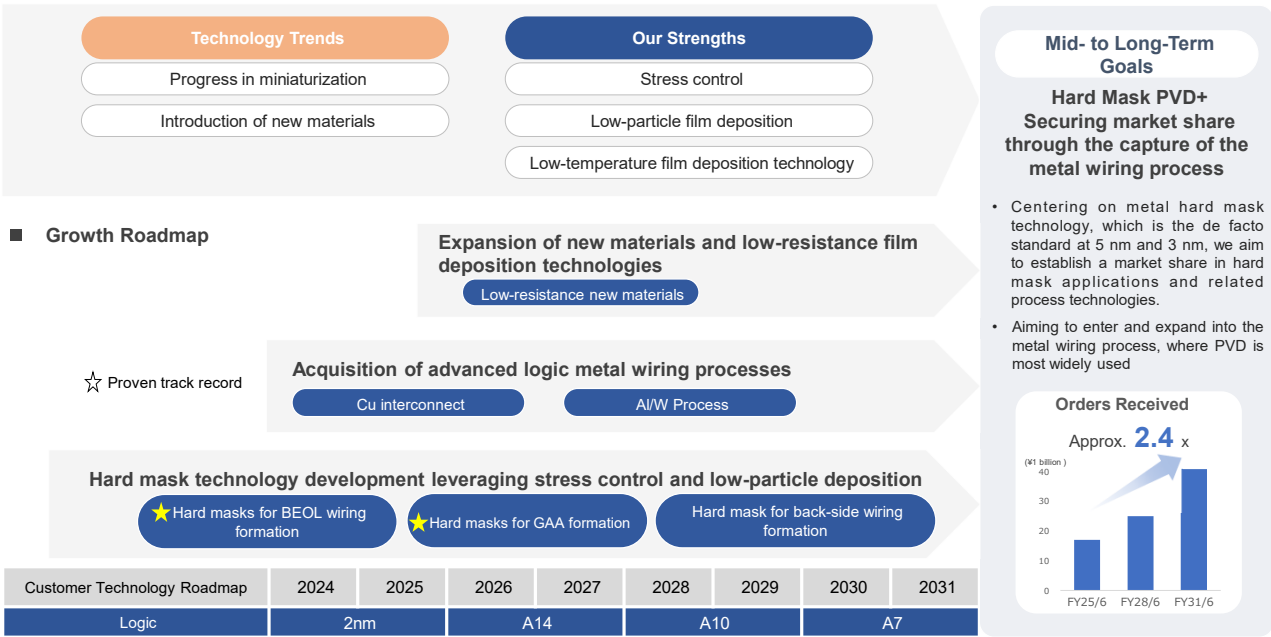
Additionally, our Semiconductors and Electronics Technology Laboratory at Fuji Susono supports customer development and also works on N+2 and beyond.

To fully cover future technologies like N+2, we participate in the Imec program in Belgium and have started process evaluation applying our a-Si HM process.

This allows us to accumulate sufficient knowledge and data before customers request it and to sense which next-generation technologies to select for development.

With these 4 R&D infrastructures—customer sites, Technology Center Pyeongtaek, Semiconductors and Electronics Technology Laboratory, and Imec—seamlessly connected, we can comprehensively cover N, N+1, and N+2 and beyond.

# Semiconductor & Logic Growth Roadmap



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This is the semiconductor and logic device roadmap shown in our new mid- to long-term management plan.

As mentioned earlier, we are expanding our lineup of hard mask equipment, a strength of ours. We continue activities to establish ULVAC as synonymous with hard mask in the market, and results are emerging.

Based on the hard mask process in the Semiconductor, we are actively investing to acquire the metal wiring process, the largest PVD process in the Semiconductor.

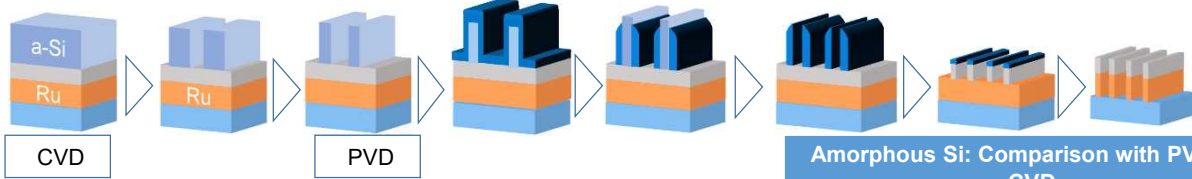
Although development of Cu wiring is taking time, our technical capabilities are steadily improving, aiming to win PORs with leading logic customers.

We are also developing deposition technologies for new low-resistance wiring materials and hard mask technologies for low-resistance wiring patterning in parallel.

# An Example of Future Technology Development for Advanced Logic

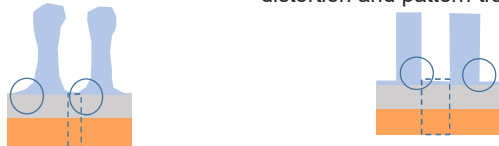


## Example of hard mask applications in Ru DME processes

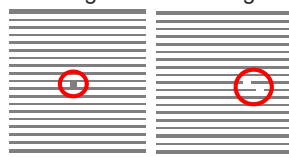


Shape distortion during trimming  
Disadvantageous during pattern transfer

Density, Si purity, low deposition temperature, low outgassing  
⇒ Superior resistance to pattern distortion and pattern transfer



Effective against microbridges and defects



Amorphous Si: Comparison with PVD and CVD		
	CVD	PVD
Deposition Temperature	High	Low
Purity	Low	High
Impurities (Hydrogen)	High	None
Hardness	Low	Mid
Film Thickness	thick	mid
Patterning accuracy	Bad	Moderate
Temperature tolerance	Moderate	High
Shape Retention	Low	Moderate
Film-forming particles	Will be Evaluated	

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Here is an example of future technology development for advanced logic. This is one of the developments and evaluations we are conducting with Imec in Belgium.

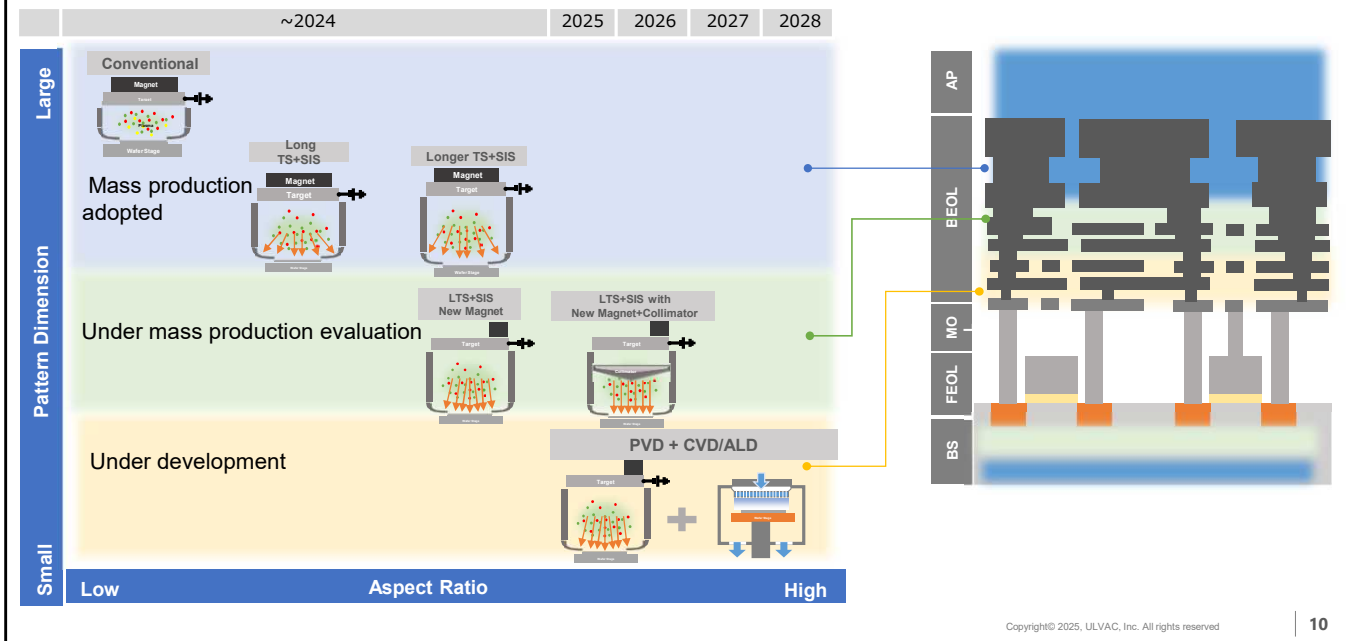
We are evaluating whether PVD a-Si has advantages as a hard mask for Ru, a low-resistance wiring material expected to be adopted in advanced devices.

Although evaluation is ongoing and results are not yet available, PVD has advantages over conventional CVD in density, Si purity, deposition temperature, and low gas emission.

This leads to better pattern shape retention during processing and superior pattern transfer, addressing customer challenges such as microbridges and defects. As shown in the comparison table on the right, PVD outperforms CVD in each category.

## Sputtering Technology for Metal Wiring Processes: Logic

» Increased opportunities through miniaturization and multilayering of interconnect layers in the logic field



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Next, I will explain Cu wiring development in the logic field. Although not yet adopted in mass production, development is steadily progressing.

The chart shows our sputtering technology and equipment lineup. The vertical axis represents the opening size of wiring patterns, and the horizontal axis is the aspect ratio (opening to depth ratio).

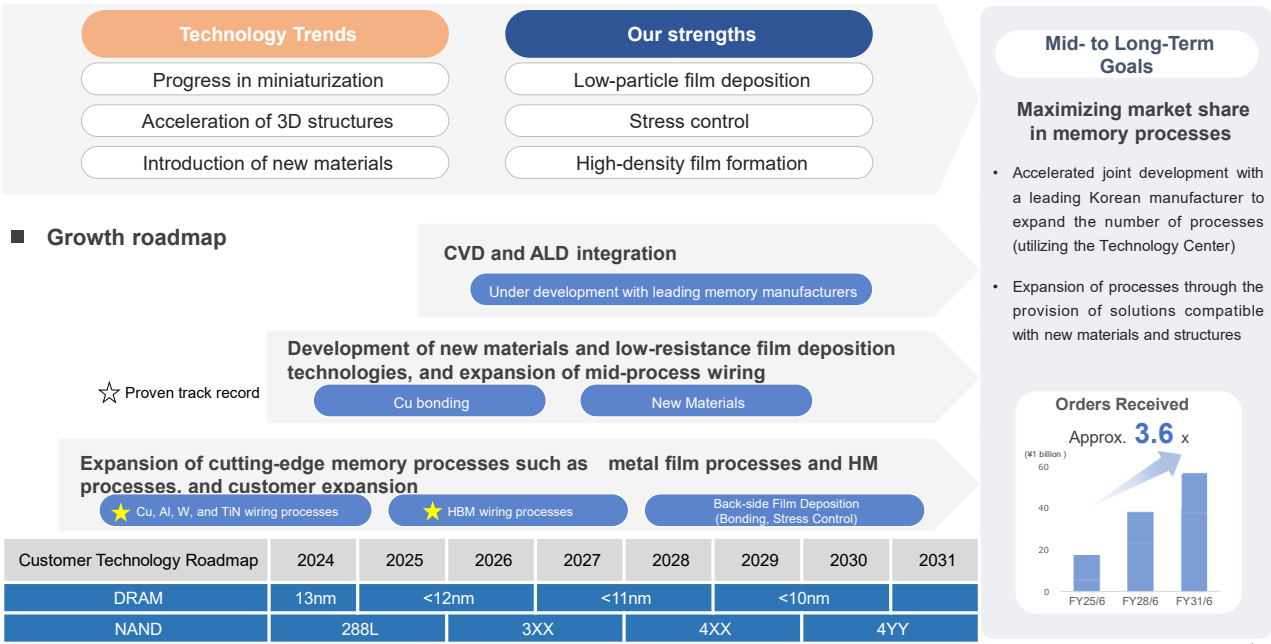
Logic Cu wiring includes various pattern shapes from relatively relaxed upper layers to more demanding middle and lower layers.

With backside power supply and further miniaturization, the total number of wiring lines will increase.

We offer conventional cathode sputtering with excellent mass production and cost performance. Also we are capable to offer Long Throw Sputtering (LTS) that increases directionality by extending the target-to-wafer distance, along with SIS modules utilizing self-sustaining discharge and ion transport technologies.

We are also developing new cathodes with improved magnets, and integration with CVD/ALD is underway. This allows us to comprehensively cover wiring from upper to lower layers and backside wiring, expanding opportunities.

# Semiconductor and Memory Growth Roadmap



This is the growth roadmap for memory devices.

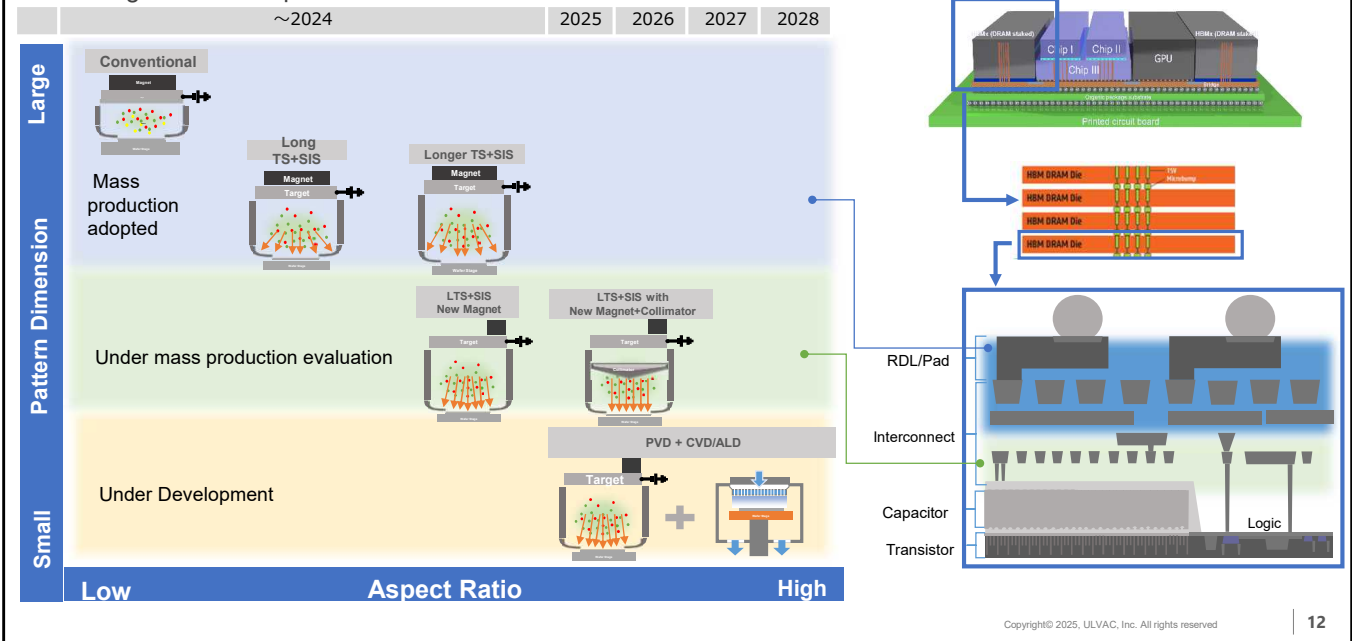
In the DRAM segment, we have mass production records for Cu B/S, Al wiring, and redistribution layers in both DDR and HBM. Last year, through joint development with a top memory manufacturer, we achieved a new POR in the metal wiring process.

We are continuing joint development with this manufacturer to expand our share in metal wiring.

Structural changes and new needs such as wafer bonding are also expanding in the memory field, and we plan to actively pursue joint development to capture these new opportunities.

# Sputtering Technology for Metal Interconnect Processes - Memory

Increased opportunities due to miniaturization and multilayering of interconnect layers in the memory field, along with the adoption of new structures such as increased total HBM count and CBA.



Although the total number of Cu wiring processes in memory is smaller than in logic, increases are expected in Cu wiring processes due to structural changes in both DRAM and NAND, such as HBM and CBA.

We will respond to these opportunities with the sputtering technology lineup explained earlier for logic.

We have also secured multiple new PORs with a major memory manufacturer in wiring processes other than Cu wiring.

## Participation in the Imec Program and Future Collaboration

- » We have participated in the program of Imec, a leading semiconductor research and development institute based in Belgium.
- » By leveraging Imec's expertise and development infrastructure, we aim to accelerate the advancement of next-generation and beyond semiconductor devices.



Finally, I would like to provide an overview of our participation in Imec's program.

As mentioned earlier, we started our participation in Q1 of FY2026 in the program of Imec, a leading semiconductor research institute in Belgium (NANO IC Program, covering MOL/BEOL).

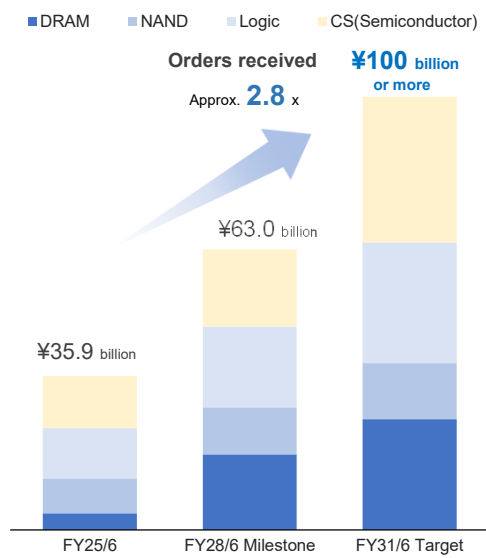
Through Imec, we will identify potential developments in future advanced logic, make appropriate selections, and allocate resources accordingly. In addition, by conducting evaluations in collaboration with Imec, we will obtain data that would be difficult to acquire on our own, and leverage it for TRMs with advanced customers.

We will also carefully assess and act upon the technological feasibility, probability of success, and market potential, while monitoring gaps between Imec's roadmap and the processes adopted by leading-edge customers.

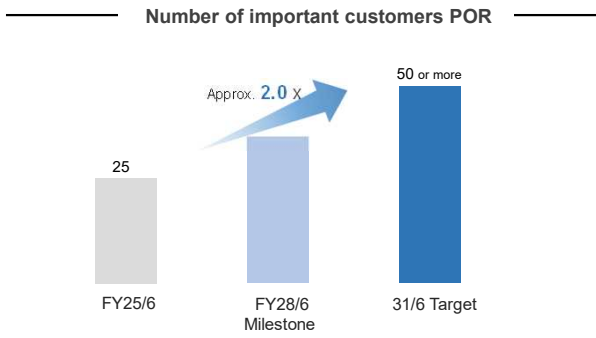
Furthermore, we intend to utilize this opportunity as a platform for fostering young engineers and for personnel exchange.

# Growth Strategy : Semiconductor Growth Scenario

» Based on proven hard mask technology and metal film deposition technology, we will increase the number of POR\*s for important customers and expand our market share by acquiring new processes, aiming for orders of ¥100 billion or more in FY31/6.



- ### Growth Strategy
- ① Apply HM (Hard Mask) technology to high-density functional films.
  - ② Establish a top position in HM processes and expand into Cu wiring applications.
  - ③ Expand PVD market share by securing advanced logic Cu wiring and post-Cu wiring processes.
  - ④ Expand and deepen the CS (Customer Support) business.



\* Process of Record: Certified process used in mass production Copyright© 2025, ULVAC, Inc. All rights reserved

By executing these initiatives, we aim to increase PORs with key customers based on our proven hard mask and metal deposition technologies, expand share by acquiring new processes, and target orders exceeding ¥100 billion by FY31/6.

# New Initiatives in Advanced Packaging

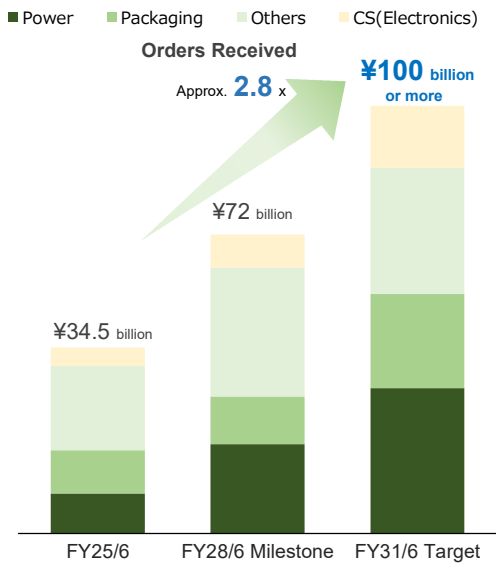
Harunori Iwai, Senior Executive Officer  
Junya Kubo, Sales Department 2  
Semiconductor and Advanced Electronics Business HQ

The ULVAC logo is displayed in a blue, sans-serif font on a light green background. The logo consists of the letters 'ULVAC' in all caps.

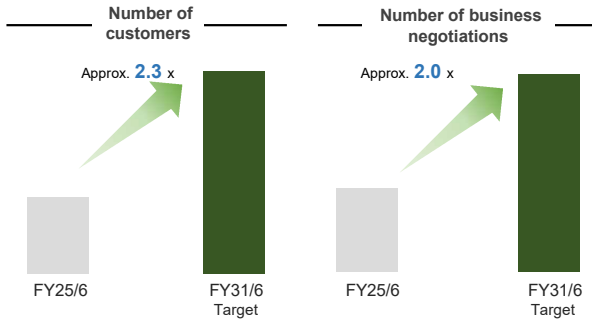
I'm Iwai. I will explain our efforts in advanced packaging.

## Growth Strategy: Growth Scenario for Electronic Devices

» We aim to expand to a business scale of over ¥100 billion and further growth mainly through the revitalization of the packaging business and the recovery of power device investments.



- Growth Strategy**
- ① Expand applications to support GaN mass production in addition to SiC sputtering and ion implantation.
  - ② Capture new processes and benefit from increased investment in advanced packaging.
  - ③ Develop optoelectronic fusion businesses through mass production of TFLN (Thin Film Lithium Niobate) etching, contributing to the miniaturization of communication devices.
  - ④ Expand and deepen the CS business.

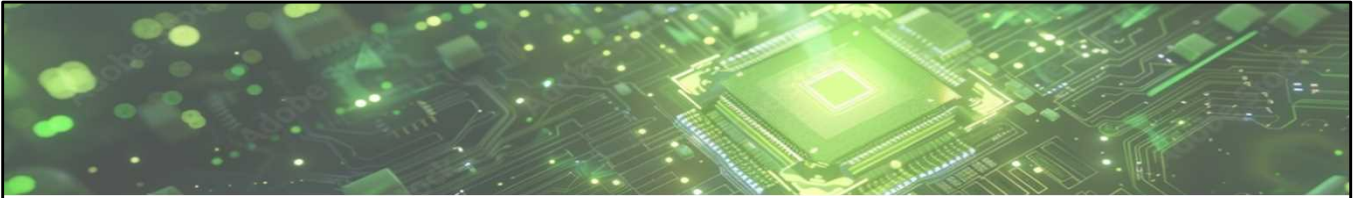


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Kondo mentioned aiming for orders exceeding ¥100 billion by FY31/6 in the semiconductor business.

In the electronics device business, we also aim for orders exceeding ¥100 billion by FY31/6.

Today, we will focus on the packaging field, where we expect significant growth.



- 1. Advanced Packaging**
- 2. Surface Treatment Technologies used in Advanced Packaging**

Speed

Cooling Capacity

Durability

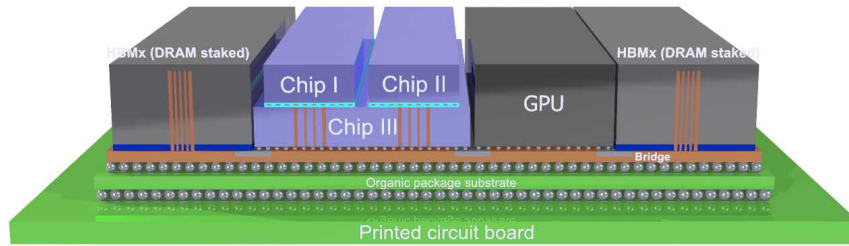
Mass productivity

AI semiconductors handle massive data and generate significant heat, so packaging innovations are essential.

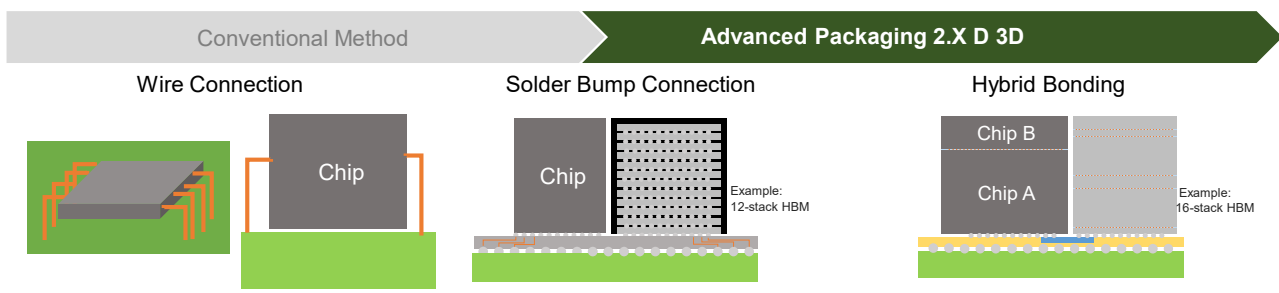
There are 4 key requirements for advanced packaging technology:

1. Speed: enabling many signals through fine wiring.
2. Cooling: efficiently dissipating heat.
3. Durability: ensuring stacked chips operate stably over time.
4. Mass production capability: producing large volumes reliably to meet global demand.

## The Role of Packaging (Fine, Short, High-Density Wiring Connections)



## Evolution of 2D/3D Packaging Technologies



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While improving chip performance is important, in AI semiconductors, how chips are arranged and stacked greatly affects the performance.

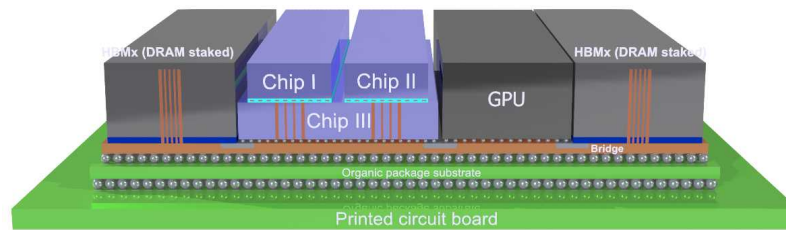
Previously, wire bonding was the mainstream for connection method.

Next, bump bonding using small solder balls became widespread.

Now, the solder balls have become even smaller for higher-density connections.

Recently, hybrid bonding, which connects chips directly without solder, has emerged.

This enables three-dimensional stacking beyond planar arrangements, significantly enhancing performance.



- |  |   |
|--|---|
| Desmear Processing for Interposers                         | Electrode formation sputtering                |
| Desmear processing for packaging substrates                | Seed sputtering for packaging substrates      |
| Etching for glass processing (optical waveguide formation) | Etching for fine patterning                   |
| TGV Glass substrate patterning                             | Plasma Dicing                                 |
| TSV Etching  | <b>Surface cleaning/hydrophilic treatment</b> |
| <b>Plasma surface activation (hybrid bonding)</b>          |   |

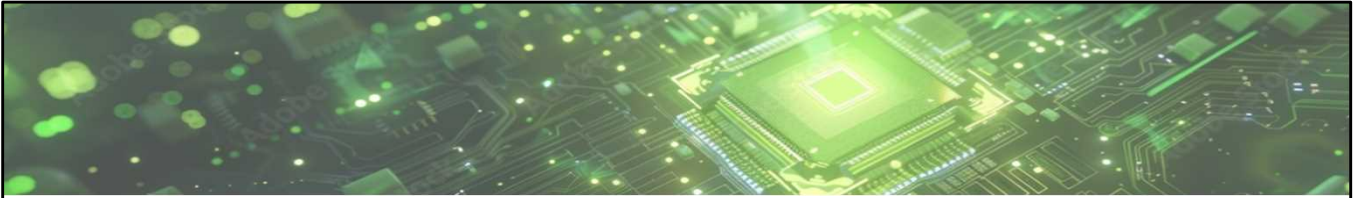
Connecting semiconductor chips requires not only the chips themselves but also very fine and precise wiring on the supporting substrates.

Our descum processing equipment and deposition equipment play active roles in creating these wirings.

Descum is already widely used, and deposition equipment usage is progressing.

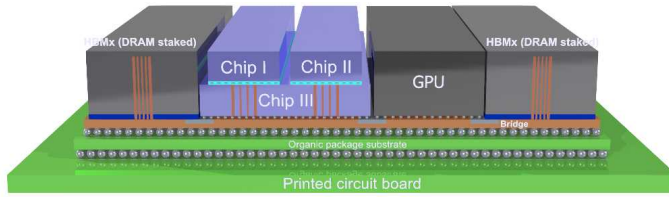
Recently, our technologies are also applied in connection areas linking chip-to-chip, chip-to-substrate, and substrate-to-substrate.

Today, Mr. Kubo will introduce our surface treatment technologies such as surface cleaning, hydrophilization, and activation.



1. **Advanced Packaging**
2. **Surface Treatment Technologies used in Advanced Packaging**

I'm Kubo. I will explain surface treatment technologies used in advanced packaging.



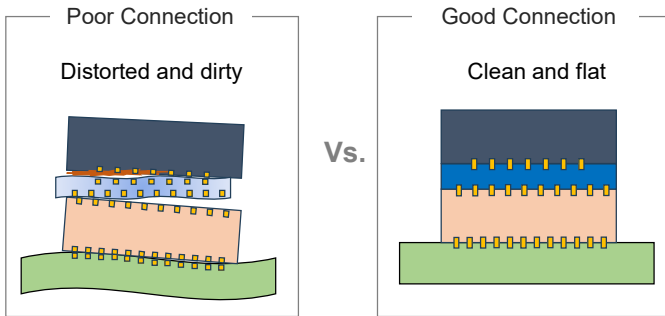
## Key Points for Multilayer Packaging

Flat Surface

Clean and good adhesion

No degradation

Efficient transfer of heat and electricity



The diagram below illustrates the concept of stacking chips in three dimensions.

Semiconductors used in smartphones and AI require stacking many small chips to operate fast and energy-efficiently.

Several conditions are necessary:

- The surface must be flat and clean.
- Materials must not be damaged and remain stable over time.
- Heat and electricity must be effectively conducted.

It is crucial that materials adhere well while maintaining ideal performance.

Meeting these conditions enables high-performance and reliable semiconductors.

Our technologies and equipment support this “stacking capability.”

3 Methods for Connecting Semiconductors: Smaller, Denser, Thinner

**Bump**

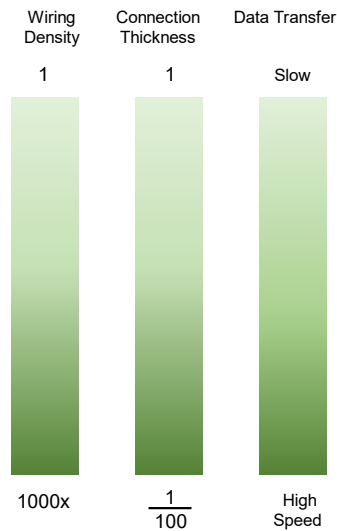
(Application Example) Board Interconnects, High-Current Applications

**Micro Bump**

(Application Example) HBM Stacked Memory

**Hybrid Bonding**

(Application Example) Next-generation HBM, Advanced 3D-IC



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This slide shows examples of connection technologies used in AI semiconductors.

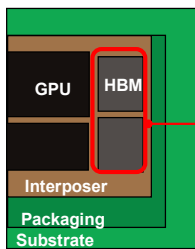
“Bump” is the basic method of connecting chips and substrates with large solder balls.

Microbump uses smaller balls for finer wiring.

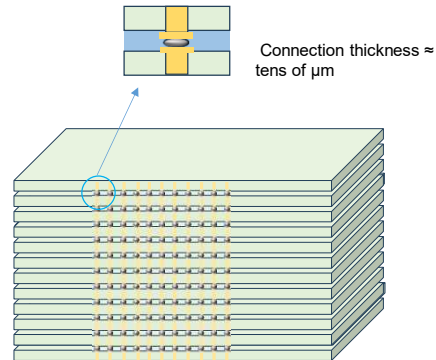
The latest “Hybrid bonding” connects electrodes directly without using solder.

This allows chips to be smaller, thinner, faster, and more energy-efficient.

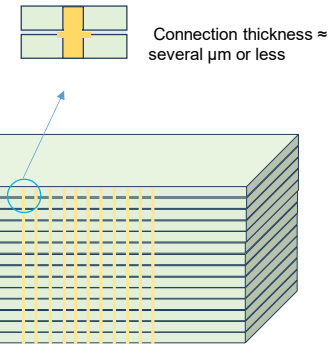
## Evolution of Connection Methods in HBM



## I. Microbump connection



## II. Hybrid bonding



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This describes the connection technology for HBM memory used in AI semiconductors.

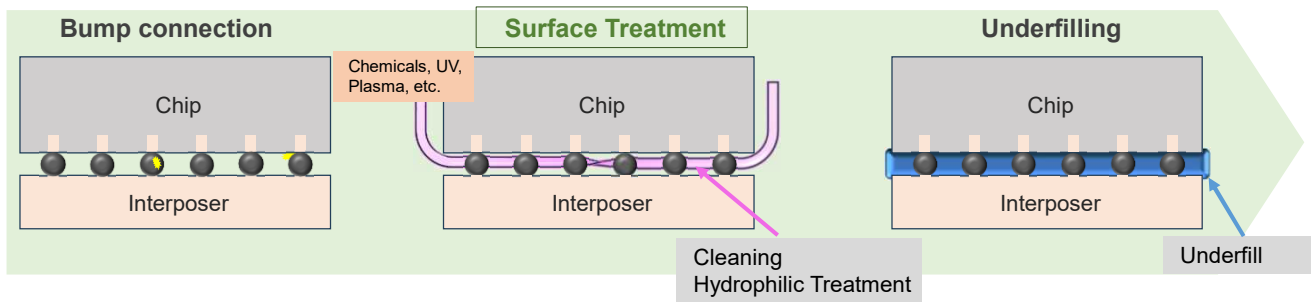
In microbump connections, chips are stacked using solder balls. The connection thickness is several tens of micrometers, which results in a relatively thick overall stack.

Next-generation hybrid bonding connects chips directly without solder, reducing the connection thickness to a few micrometers or less. This enables thinner stacks with more memory layers, allowing faster and more energy-efficient operation.

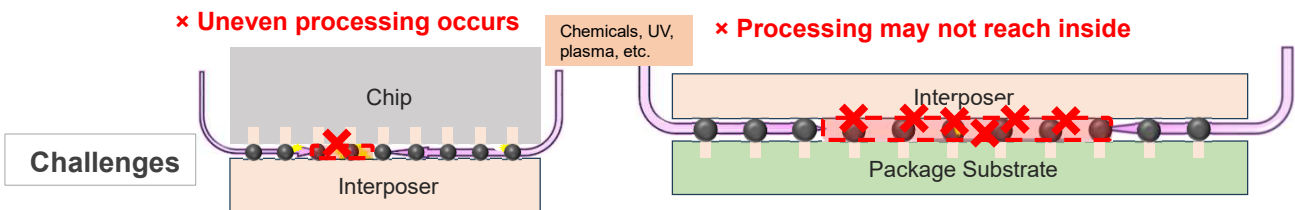
Our surface treatment technology plays a vital role in these areas.

Now, I will introduce our surface treatment technology used in microbump connections.

Surface treatment to stabilize bump connections



As chip and substrate gaps narrow and sizes increase in the future,



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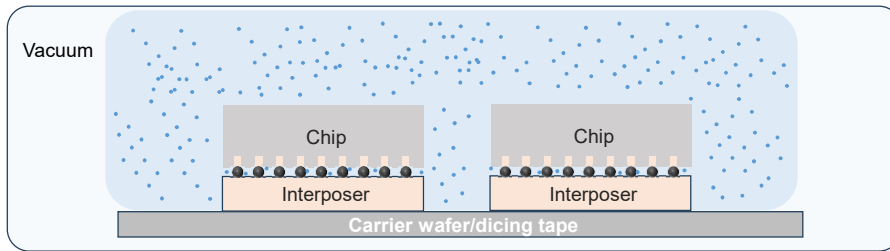
When connecting chips with bumps or microbumps, underfill resin is injected for strength and heat dissipation.

The surface treatment before resin injection is critical to ensure stable resin flow inside.

However, as wiring becomes finer and substrates larger, uneven surface treatment can cause resin to fail to spread thoroughly, risking unstable connections.

Therefore, surface treatment processes such as hydrophilization and cleaning are increasingly important.

## Our Process: Vacuum + Radicals



Radical: Immediately disappear by highly reactive collide

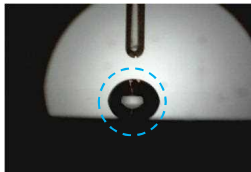
Vacuum: Maintains radical effectiveness by prevents unnecessary collisions.



Our Process Equipment

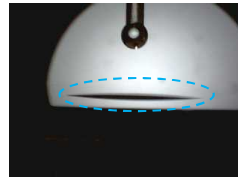
## What is hydrophilic treatment?

Before



Making the surface water-repellent

After



to a state where water adheres

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We use vacuum plasma technology to efficiently generate radicals, enabling uniform and strong connections.

Radicals are highly reactive particles that quickly disappear in the atmosphere but remain stable and spread in the vacuum environment, reaching deep into narrow gaps.

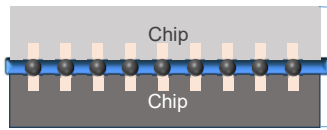
Hydrophilized surfaces change from repelling water droplets (left diagram) to attracting water (right diagram).

By making surfaces more water-friendly, resin spreads thoroughly, enabling stable connections.

This ensures chips are firmly connected and semiconductors operate stably over time.

## Hybrid Bonding Applications and Challenges

### I. Microbump Connection

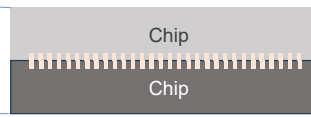


#### Advantages

- Increased wiring density
- Thinner due to bump thickness

**Expected for application in high-performance semiconductors**

### II. Hybrid Bonding



#### Challenges

- High-precision surface treatment and alignment required
- Process optimization for mass production is a challenge

**Expectations for process optimization toward mass production**

**Equipment optimization and mass production verification are required for packaging applications**

Next is hybrid bonding.

This method allows finer and denser wiring, enabling smaller, more efficient chips.

It is expected to be essential for future high-performance semiconductors.

In fact, it is already used in CMOS image sensors for cameras.

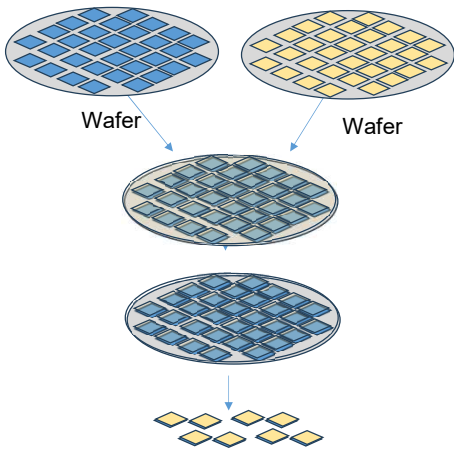
The semiconductor industry is further improving its precision.

Going forward, research is underway to optimize equipment and processes for packaging semiconductors, ensuring long-term stable use.

We are now preparing for the future mass production.

Types of hybrid bonding

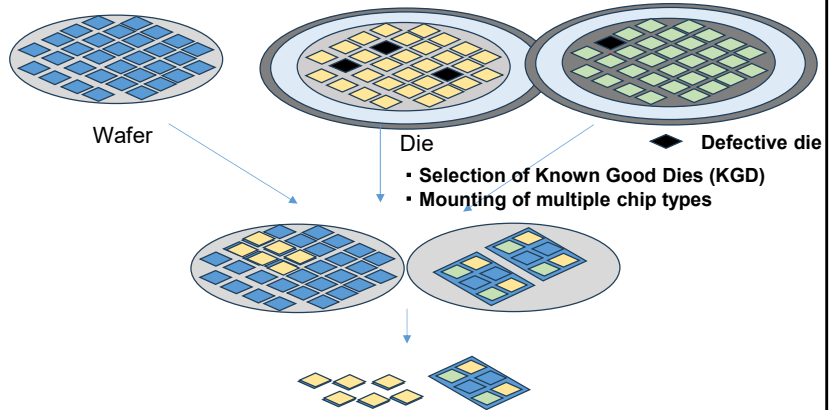
W to W (Wafer to Wafer)



Capable of attaching many chips at high speed  
Mature and still evolving

D 2 W (Die to Wafer)

Our Focus



Good chip sorting and heterogeneous chip combination possible  
Mass production development is progressing

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There are two main hybrid bonding methods.

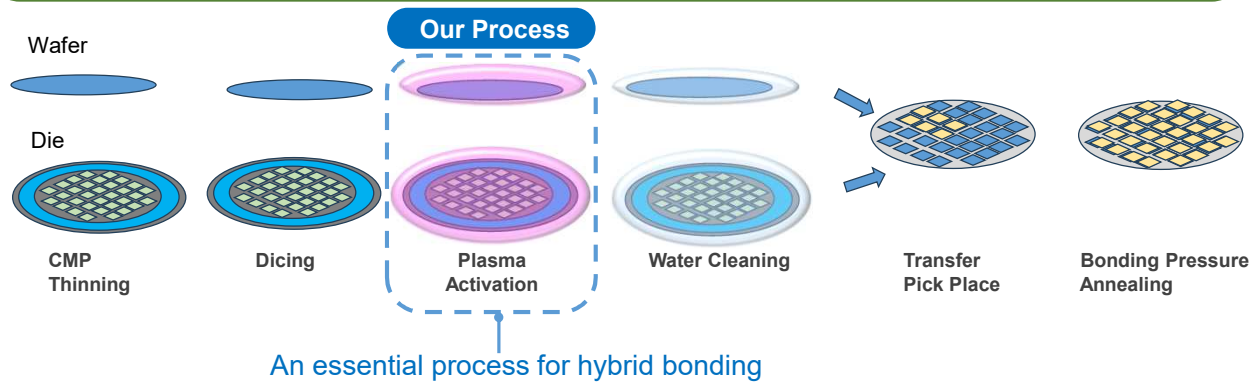
One is Wafer-to-Wafer (W2W), bonding the entire wafers at once. It is a mature technology capable of high-speed processing of many chips, with ongoing miniaturization and precision improvements.

The other, highly anticipated method is Die-to-Wafer (D2W), bonding individual chips after dicing.

This allows selection of only accepted chips and combining different chip types.

We are focusing on the essential process of the D2W process hybrid bonding method, which we consider a critical growth area supporting the mass production of next-generation semiconductors.

**D2W Bonding**



**Our Strength**

- Improve substrate surface reaction with using gentle plasma
- Dedicated equipment capable of uniformly processing individual chips

Our focus is on the surface activation process essential for hybrid bonding.

Surface activation uses plasma to treat surfaces, increasing reactivity for adhesion.

Using vacuum technology keeps surfaces clean, ensuring bonding reliability and process stability.

The important point is not to complete the process with a single dedicated equipment alone, but to optimize it in harmony with the preceding and subsequent processes.

In addition to extensive surface treatment experience, we have element technologies for D2W equipment using dicing tape frames instead of wafer handling, which is also a strength.

Having these technologies allows customers to significantly shorten development time and minimize risks in product launch and mass production.

**Our Advantage for Bump Connection**

Smaller Scale

Hydrophilicity

Dicing Frame Compatibility

Radical Treatment

**Our Advantage for Hybrid Bonding**

D2W

Activation

Dicing Frame Compatibility

Plasma Control

**Roles of ULVAC**

Optimal Surface Treatment



Stable Equipment Supply

Our role has two main aspects.

One is providing the “process to optimally prepare surfaces before bonding,” using technologies like hydrophilization, radical treatment, and activation to create surfaces that bond stably.

The other is, as an equipment manufacturer, reliably supplying this technology to mass production sites.

Having a mass production system capable of this is our strength.

Providing equipment that can be safely used in actual production, not just research, is our great value.

By balancing these two aspects, we will support the advancement of advanced packaging and correspond to the growing market needs.

# Strengths and Future Development of Surface Analysis System

Hirohisa Takahashi  
Executive Officer, President and Representative Director, ULVAC-PHI, Inc.  
Takuya Miyayama  
Senior Manager, Product Strategy Department, ULVAC-PHI, Inc.

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I'm Takahashi, President of ULVAC-PHI.

We will introduce ULVAC PHI's initiatives, which we expect to grow as a Semiconductors and Electronics-related business.

We have prepared a brief introductory video of just under two minutes. Please watch that first.

[CLICK HERE](#)

**PHI Gr.**

- **AES** Auger Electron Spectroscopy, **XPS** X-ray Photoelectron Spectroscopy, **SIMS** Secondary Ion Mass Spectrometry (TOF-SIMS, Q-pole-SIMS) **The world's only company** possessing all three surface analysis techniques (Hardware, Software)
- A leading surface analysis instrument manufacturer with **a strong track record of actual deliveries to national research institutes and top global companies** (over 2,000 units delivered, over 1,300 units in operation)
- ULVAC-PHI will leverage its XPS technology cultivated through surface analysis instruments for research and development to challenge the commercialization of XPS inspection equipment for semiconductor mass production lines by FY27/6, aiming to become a world-leading company in both analytical instruments and inspection equipment.

Auger electron spectroscopy (AES)



PHI 710

X-ray photoelectron spectroscopy (XPS)



PHI GENESIS

Secondary ion mass spectrometry (TOF-SIMS)



PHI nanoTOF 3+

Secondary ion mass spectrometry (Q-pole-SIMS)



PHI ADEPT1010

Let me first introduce ULVAC-PHI.

We are the only company in the world that offers three surface analysis techniques—AES, XPS, and SIMS—in one company.

Our products are analytical instruments capable of obtaining data and information from just a few nanometers of solid surfaces, mainly used in R&D.

We have a strong track record delivering to national research institutes and top global companies, holding the top share in R&D surface analysis instruments.

We aim to leverage the core technologies cultivated in R&D instruments to commercialize semiconductor inspection equipment.

## History

### May, 1969

PHYSICAL ELECTRONICS (PHI) founded by Dr. R. E. Weber of the University of Minnesota

- Developed the world's first commercial AES surface analysis instrument Subsequently added XPS and SIMS to its product lineup, establishing its position as a surface analysis supplier



Founder  
Dr. R. E. Weber  
University of Minnesota

### April, 1971

Nippon Vacuum Technology Co., Ltd. (now ULVAC, Inc.) signed an exclusive agency agreement with PHI

### November, 1982

PHI and Nippon Vacuum Technology Co., Ltd. established the joint venture ULVAC-PHI Co., Ltd.

### February, 2003

Acquired the Surface Analysis System business division from PHI and commenced manufacturing and global sales of surface analysis instruments

### November, 2023

Established a new company, ULVAC PHI Instruments, in China

### Present

Operating globally through three companies: ULVAC-PHI (Japan), PHYSICAL ELECTRONICS (U.S.), and ULVAC PHI Instruments (China)

Our company originated from Physical Electronics, the first to commercialize AES surface analysis instruments worldwide.

Since then, we have developed XPS and SIMS instruments as a surface analysis equipment manufacturer.

In 2003, we joined the ULVAC Group and now operate globally mainly through three companies in Japan, the US, and China.

### Value Proposition

Through analytical technologies that "convert the invisible into data and information", we provide critical data and information that supports customers' decision-making.

### Strengths

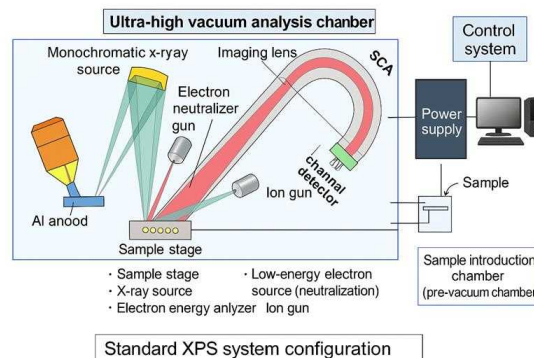
① Technology featuring high-precision, wide-ranging surface analysis techniques

Surface analysis methods of competitors		ULVAC	A	B	C	D	E
Analysis Method	XPS X-ray Photoelectron Spectroscopy	●	●	●	●		
	AES Auger electron spectroscopy	●			●		
	SIMS Secondary Ion Mass Spectrometry					●	
	TOF-SIMS Top Surface Analysis	●					
	D-SIMS Depth Analysis	●					●

Excerpt from FY24.6 Q4 Financial Results Disclosure Materials

② Total coordination of analytical instruments

- Hardware: Challenging detection limits
- Software : Converting signals into data and information
- System: Integrated Value Chain



Our value proposition is by utilizing cutting-edge surface analysis technology to “Convert the invisible into data and information,” we provide critical data and insights that support our customers’ important decisions in new discoveries, innovation, quality control, and failure analysis.

Our strengths are:

We have a broad range of surface analysis techniques, enabling highly precise data acquisition and utilization compared to competitors.

We offer total coordination of surface analysis, continuously challenging detection limits in hardware and converting obtained signals into usable data and information using physics and mathematics in software.

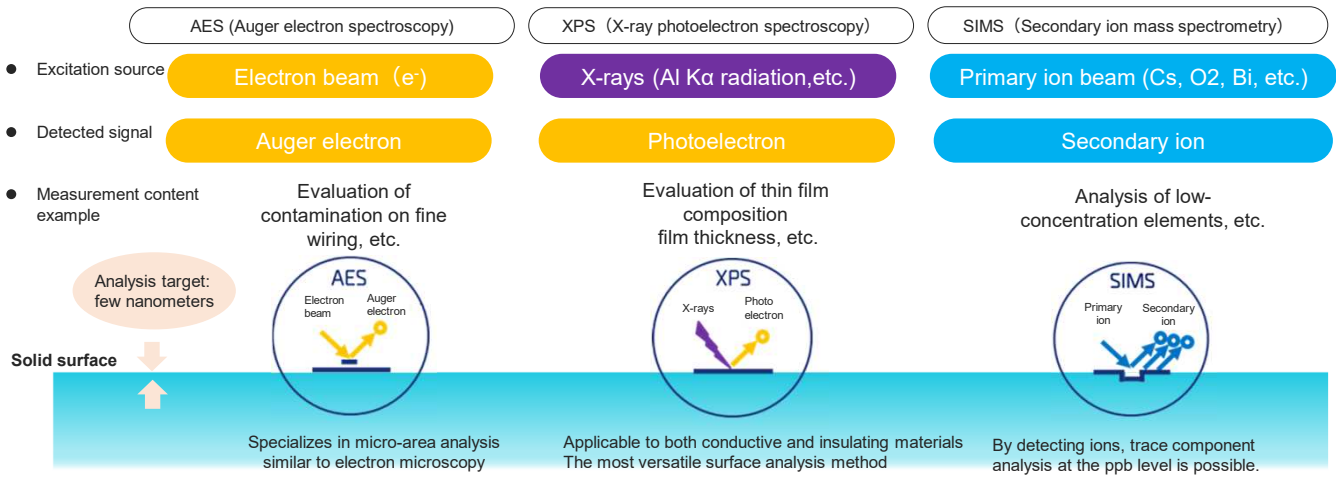
We provide all these functions seamlessly across the entire value chain, from R&D through manufacturing and after-sales service.

From the next page, our Marketing Manager, Mr. Miyama, will explain the advantages and benefits of surface analysis.



## Core Technology: What is Surface Analysis

- » Analysis of elemental composition, chemical states, and molecular structure in the surface region at the nanometer scale
- » A technique that enables material evaluation by combining two-dimensional distribution observation (imaging) and depth profiling analysis.



I'm Miyama. First, I will explain our core technology: surface analysis.

Surface analysis examines an extremely thin layer—just a few nanometers—on solid surfaces, revealing which elements are present, their chemical states, and even molecular structures. It can also visualize the two-dimensional distribution of elements at specific locations, showing where and how much of each element exists as images.

Furthermore, it can analyze how components change from the surface into the material's interior.

By combining these capabilities, surface analysis provides detailed evaluation of material properties and conditions.

The three main techniques we offer are Auger Electron Spectroscopy (AES), X-ray Photoelectron Spectroscopy (XPS), and Secondary Ion Mass Spectrometry (SIMS).

AES irradiates the sample surface with an electron beam and detects emitted Auger electrons.

Because it uses a finely focused electron beam like an electron microscope, it is suitable for evaluating surface contamination and foreign material distribution on the very top layer.

XPS irradiates the material with X-rays and detects emitted photoelectrons, enabling determination of elemental composition and distribution on solid surfaces.

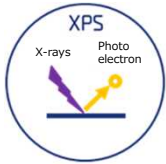
It is the most versatile surface analysis technique, applicable to conductive and insulating materials alike.

SIMS irradiates the surface with primary ions and detects emitted secondary ions.

Unlike AES and XPS, SIMS uses ion beam sputtering, making it a destructive analysis method.

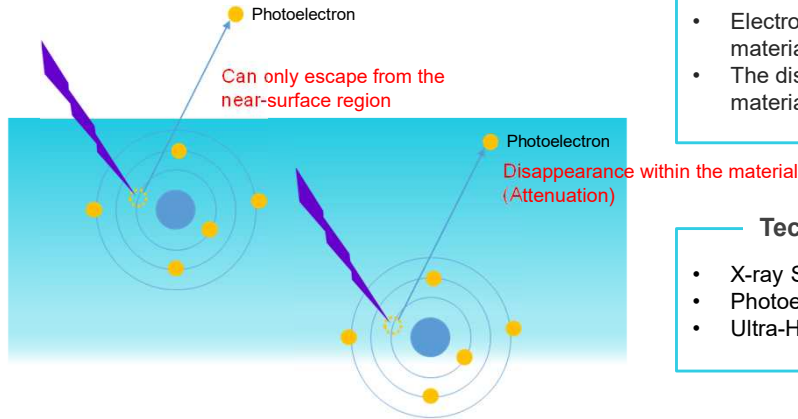
Its key feature is the ability to detect trace elements at parts-per-billion (ppb) levels by analyzing ions.

On the next page, I will explain XPS in detail, which is used for measuring film thickness on the nanometer scale.



**XPS (X-ray Photoelectron Spectroscopy)**

An analytical method that utilizes the photoelectric effect, in which electrons are emitted from a material when it is irradiated with X-rays.



**The reason why XPS is a surface-sensitive technique**

- Electrons lose energy and attenuate within the material.
- The distance electrons can travel within the material is at most a few nanometers.

**Technologies Required for XPS**

- X-ray Source
- Photoelectron Analyzer
- Ultra-High Vacuum (Ulvac's Core Technology)

XPS, or X-ray Photoelectron Spectroscopy, is an analytical method that irradiates a solid surface with X-rays and utilizes the photoelectric effect, where electrons are emitted from the material.

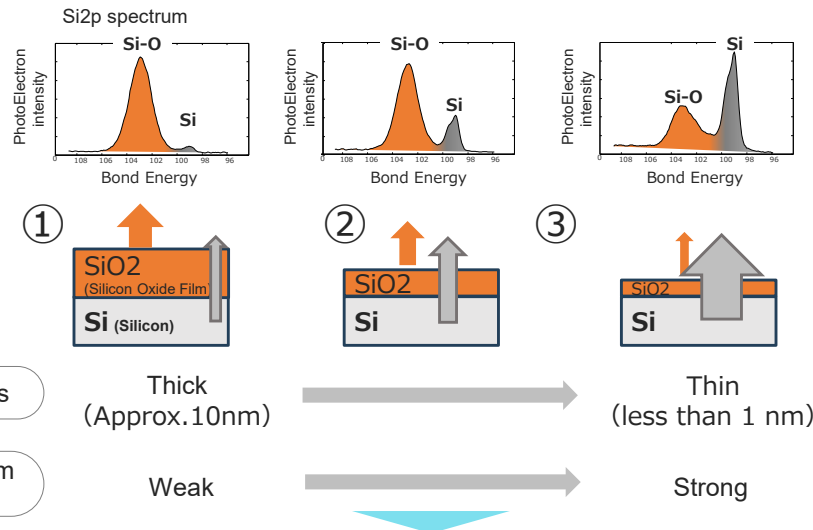
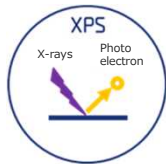
By measuring the energy of these emitted electrons, we can identify the elements present on the surface and their chemical states.

As the emitted electrons travel through the material, they lose energy by colliding with other atoms and electrons—a process called attenuation.

Because of this, the distance electrons can travel inside the material is very short, limited to a few nanometers.

Therefore, the electrons detected originate from very near the surface, making XPS a powerful surface analysis technique.

Key technologies for XPS include the X-ray source as an excitation energy source for electrons, the photoelectron analyzer that measures their kinetic energy and ULVAC's core technology of ultra-high vacuum systems that maintain the necessary vacuum conditions.



Thickness evaluation possible for **thin films below 10 nm**

Here is an example of thin film measurement using XPS. For instance, when measuring the thickness of a silicon oxide film deposited on a silicon wafer, the photoelectrons from the silicon substrate and the silicon oxide film have slightly different energies, even though both originate from silicon atoms.

By exploiting this energy difference, we can distinguish the chemical states of the substrate silicon and the surface silicon oxide.

The intensity of each signal changes depending on the thickness of the silicon oxide film.

Using this relationship, XPS can accurately measure silicon oxide films only a few nanometers thick.

The diagram below illustrates this concept:

- ① When the silicon oxide film is thick, the signal from the oxide dominates.
- ③ When the film is thin, the oxide signal weakens, and the substrate silicon signal becomes stronger.

XPS can precisely measure film thicknesses below 10 nm by utilizing this phenomenon.

Some detection methods cannot measure such thin films due to insufficient sensitivity, but XPS can.

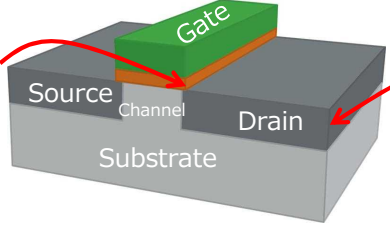
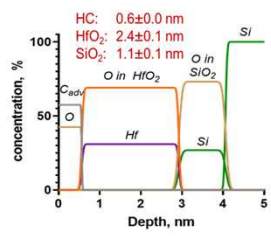


Transistor (FEOL)



**XPS**  
Non-destructive compositional evaluation of gate oxide film thickness

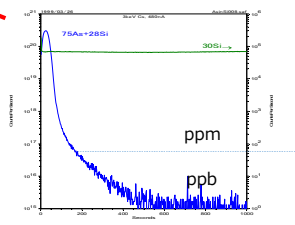
- ✓ Film thickness evaluation of a few nanometers



**SIMS**  
Ion Implanter evaluation for source/drain formation

- ✓ ppb-level dopant evaluation

Evaluation and measurement of extremely trace amounts of dopants (impurity elements)

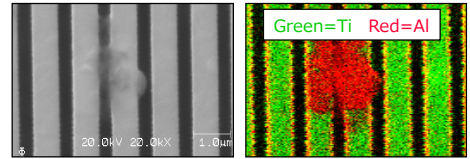


Wiring (BEOL)



**AES**  
Contamination/foreign matter evaluation of the trench area

- ✓ Micro-area analysis similar to electron microscope observation
- ✓ Evaluation of contamination/foreign substances on the extreme surface layer



Surface analysis is indispensable for evaluating increasingly miniaturized and advanced semiconductors.

XPS can non-destructively measure the thickness of gate oxide films in transistor regions of logic and memory devices.

SIMS, which detects ions scattered by ion irradiation, can evaluate trace dopants and impurities, enabling assessment of ion implantation in source and drain formation.

AES, using electron beams, can examine contamination and foreign materials in wiring trenches with spatial resolution comparable to electron microscopes, detecting even very thin surface contaminants.

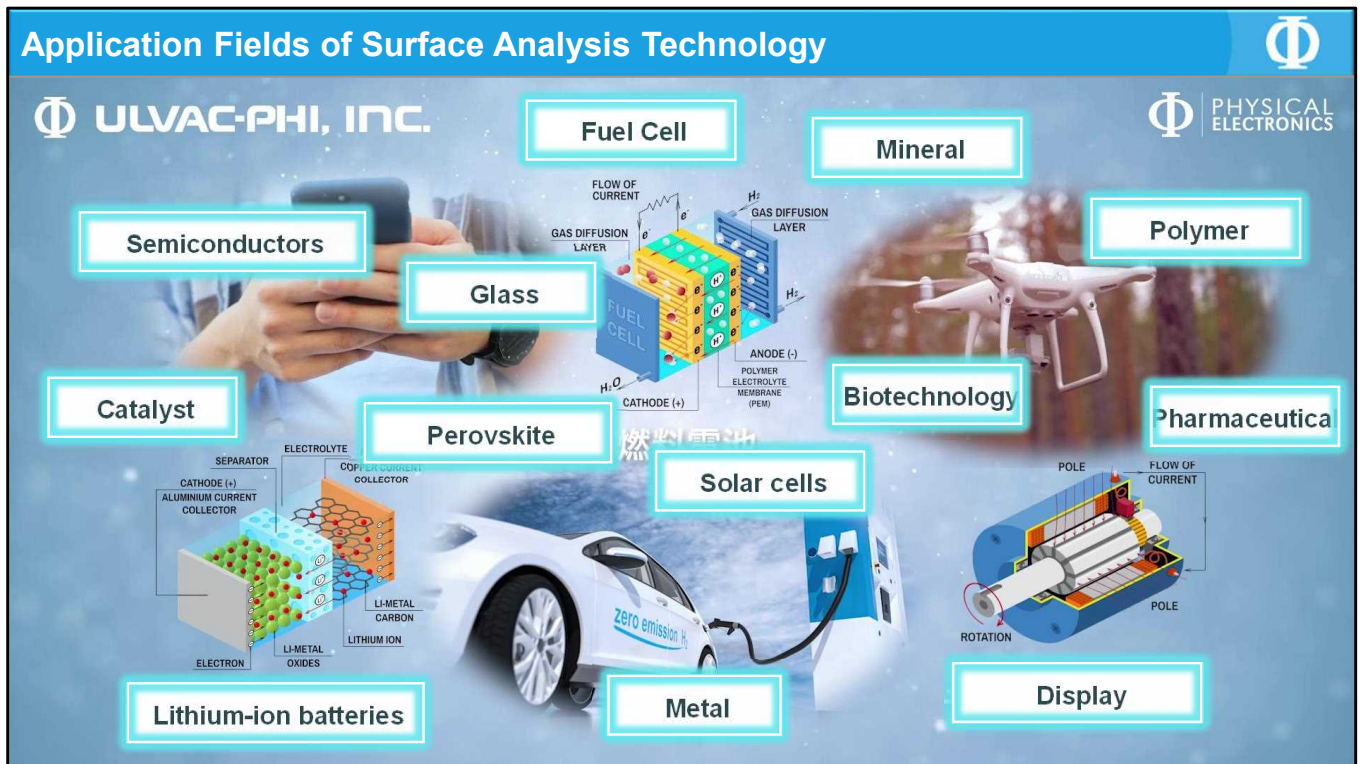
Thus, our surface analysis technologies support diverse evaluations throughout semiconductor manufacturing processes, meeting the rising precision demands driven by miniaturization and complexity, and making significant contributions.

# Application Fields of Surface Analysis Technology



ULVAC-PHI, INC.

PHYSICAL ELECTRONICS



Surface analysis technology is widely used beyond semiconductors, across many industries.

As Mr. Takahashi explained earlier, by leveraging cutting-edge surface analysis technology to “turn the invisible into data and information,” we contribute to industrial advancement.

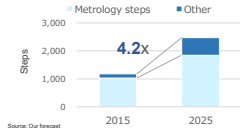
This concludes my explanation. I will now hand back to Mr. Takahashi.

# Challenge from Lab to Fab

» Leveraging experience and achievements in the existing Lab-type model (market share No. 1), we aim to establish a global position in the inspection equipment market by fully introducing "XPS" into the Fab-type model, where the importance of analysis increases due to the advancement of manufacturing processes, through synergies between semiconductors and electronics and other

## Market Environment

The semiconductor manufacturing process has doubled in the past 10 years, with the inspection process increasing fourfold.



## Technology and Market Trends

- Increase in process steps due to advances in miniaturization
- Growing demand for yield improvement
- Increased importance of quality control

## Our Strengths

- Our track record as surface analysis specialist manufacturer
- R&D to service integrated system
- Providing value from both Software (Science) /Hardware (Physical and Optical Design, Manufacturing)

### by FY25/6

#### Top share in XPS analysis equipment for research and development

- Expansion of XPS analysis equipment for research and development
- Prototype development of XPS inspection equipment for semiconductor mass production lines



XPS analysis equipment for research and development

### by FY27/6

#### Market launch of XPS inspection equipment for semiconductor mass production lines

- Improvement of XPS analysis equipment for research and development
- Product release of XPS inspection equipment for semiconductor mass production lines

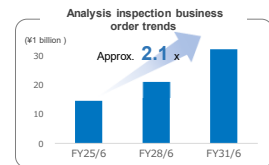


XPS inspection equipment for semiconductor production lines Image

### by FY31/6

#### Aiming for further expansion through scaling global operation

- Expansion of the lineup of analytical instruments for research and development
- Expansion of production capacity for XPS inspection equipment for semiconductor mass production lines
- Commercialization of a business generating **¥30 billion** in orders for analytical instruments and inspection devices







Analytical inspection equipment is expected to grow further.

We have secured No.1 share in XPS analytical equipment for R&D, and going forward, leveraging synergies with the semiconductors and electronics business, we aim to launch XPS inspection equipment for semiconductor mass production lines.

By accelerating these initiatives, we plan to grow this business to approx. ¥30 billion by FY31/6, establishing a new pillar in the semiconductors and electronics-related business.



	Analytical Instruments	Testing Equipment
Takt Time	Not specified	Required
Measurement Target (Materials/Composition)	Unknown	Known
Measurement Method	Destructive	Non-destructive
		
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As I have repeatedly mentioned, our business has been focused on analytical instruments.

While the core technologies used in analytical instruments and inspection equipment are the same, their device requirements differ.

Analytical instruments have no takt time constraints, but inspection equipment must measure a set number of samples within a given time.

Analytical instruments detect broadly to identify unknowns, whereas inspection equipment confirms film thickness and composition based on known structures.

Regarding inspection methods, analytical instruments can destructively analyze small samples, but inspection equipment must be non-destructive to verify during manufacturing processes, as mentioned earlier.



We are aiming to realize XPS inspection equipment for semiconductor mass production lines by combining both companies' assets



**Business Synergy**

XPS Inspection Equipment for Semiconductor Mass Production Lines

Release in FY27/6

Aiming for commercialization of a ¥30 billion-scale business in analytical instruments and inspection equipment by FY31/6

Seamless provision of data and information from R&D (analytical instruments) to mass production (inspection equipment)  
Solutions for production equipment and inspection equipment

To meet the requirements for inspection equipment, we combine ULVAC-PHI's core surface analysis technologies with the semiconductors and electronics BU's hardware capabilities, including 300mm wafer handling, low particle, and takt time technologies essential for inspection systems.

By leveraging the synergy of these technologies, we aim to realize inspection equipment that maximizes the performance of our surface analysis technologies.

If this project succeeds, ULVAC-PHI will be able to provide seamless data and information from R&D to mass production.

By offering solutions both in production equipment through ULVAC Semiconductors and Electronics Devices and inspection equipment through ULVAC-PHI, we aim to establish a strong position for the ULVAC Group in the semiconductor industry.

**ULVAC**